PANJAB UNIVERSITY, CHANDIGARH-160014 (INDIA)
(Estd.under the Panjab University Act VII of 1947-enacted by the Govt. of India)

FACULTY OF ENGINEERING & TECHNOLOGY

SYLLABI

AND THE

REGULATIONS

FOR

M.Tech. (Microelectronics)
2016-17

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# Scheme of Examination for Master of Technology (Microelectronics) 2016-17

## First Semester

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Subject Name</th>
<th>L-T-P</th>
<th>Contact hrs/week</th>
<th>Credits</th>
<th>Marks</th>
<th>Practical*</th>
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<tr>
<td>1</td>
<td>MIC 6101</td>
<td>Semiconductor Device physics</td>
<td>3-0-2</td>
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<td>MIC 6102</td>
<td>Integrated Circuit Technology.</td>
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<td>MIC 6103</td>
<td>MOS Integrated Circuit Modeling.</td>
<td>3-0-2</td>
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<td>4</td>
<td>MIC 6105</td>
<td>Hardware Description Languages and VLSI Design.</td>
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<td>Elective- I</td>
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<td>MIC 6108</td>
<td>Research Seminar- I</td>
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* Practical marks are for continuous and end semester evaluation

**Total Marks: 800**  
**Total Credits: 21**

**Elective-I**

- MIC 6104 Computer Aided Design Methodologies and Tools.
- MIC 6106 Material Science & Engineering.
- MIC 6107 Embedded System Design.
## SECOND SEMESTER:

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<th>S. No.</th>
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<td>MIC 6202</td>
<td>Measurement and Characterization Techniques.</td>
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<td>5</td>
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<td>MIC 6203</td>
<td>Architecture of VLSI System.</td>
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<td>5</td>
<td>3+1</td>
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<td>Analog and Mixed Signal Device Design.</td>
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* Practical marks are for continuous and end semester evaluation

**Total Marks: 800**

**Total Credits: 21**

### Elective- II

- MIC 6206  MEMS and Microsystems.
- MIC 6207  RF and High Speed Digital Design.
### THIRD SEMESTER

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* Practical marks are for continuous and end semester evaluation

**Total Marks: 400**

**Total Credits = 18**

#### Elective- III
- MIC 7102 Microelectronic Packaging and Testing
- MIC 7103 Nano Scale Devices and Systems

### FOURTH SEMESTER:

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* Practical marks are for continuous and end semester evaluation

**Total marks: 200**

**Credits = 15**

**Internal Assessment of Thesis (ECE 7201) will be graded as follows:**

<table>
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<th>Grade</th>
<th>Requirement</th>
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<tr>
<td>1.</td>
<td>A+</td>
<td>Publication from Thesis in SCI/SCIE indexed Journal</td>
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<tr>
<td>2.</td>
<td>A</td>
<td>Publication from Thesis in Scopus/ESCI indexed Journal</td>
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**Total M.TECH. Marks: 2200**

**Total M.E. Credits: 75**
SYLLABUS

COURSE CONTENTS FOR M.TECH (MICRO-ELECTRONICS)

1ST SEMESTER

MIC 6101: SEMICONDUCTOR DEVICE PHYSICS

Max. Marks: 50

Credit Theory : 3
Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

PART-A


PART-B

Bipolar Transistors: BJT action, minority carrier distribution, low frequency CB current gain, equilibrium circuit Models, Junction field effect transistor: JFET concepts, device characteristics, nonideal effects, equivalent circuit and frequency limitation, Metal oxide Semiconductor field effect transistors: Metal semiconductor ohmic contacts, MOS structure and operation, capacitance-voltage characteristics, small signal equivalent circuits, nonideal effects.

References:
4. MOS Field Effect Transistor and Integrated Circuits by Paul Richaman, John Wiley and Sons.
MIC 6102: INTEGRATED CIRCUIT TECHNOLOGY

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

- Crystal growth and wafer preparation, defects, clean room concept, wafer cleaning techniques.
- Oxidation diffusion, Epitaxy, Ion Implantation, Metallization, Lithography, Etching.
- Typical Bipolar and MOS device fabrication techniques.
- Integration of unit processes, process modeling, IC Packaging, Reliability and failure analysis.

References:

5. Silicon VLSI Technology, James D. Plummer and Michael D. Deal Pearson Education. 2001

Practical:

1. Introduction to process simulation tools, e.g. SUPREM, MINIMOS, STEPS etc.
2. Simulation of typical MOS processes and MOSFET Characteristics, extraction of parameters for circuit simulation.
MIC 6103: MOS INTEGRATED CIRCUIT MODELLING

Credit Theory : 3
Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

- Characteristics of MOS digital circuits, Inverters, NMOS NOR and NAND gate logic circuits.
- CMOS Logic gates, transmission gates, signal propagation delays, Noise in Digital logic circuits.
- Random Logic vs. standard logic forms, PLA Structured gate layout.
- Clocking systems, clocked CMOS logic, semiconductor memories.
- Microprocessor design, Device modeling, Circuit modeling.

References:
2. Introduction to VLSI Systems, Mead and Convey, Addison Wesley. 1982

PRACTICALS

- Simulation using schematic editor
- Schematic page editor. Part editor, programmer’s editor,
- Session Log editing properties- spreadsheet editor property editor.
- Hierarchical design- Hierarchical blocks, ports, pins
- Placing, editing and connecting parts
- Editing and adding graphics
- Configuring a macro
- Creating a netlist
- Exporting and importing schematic data
• Analog stimuli-VSTIM, ISTIM
• Editing and creating models
• Digital simulation-Digital simuli DIGLOCK
• Simulation Parameters
• D.C Sweep Analysis
• Transient Analysis
• AC Sweep Analysis
• Parametric Analysis
• Performance Analysis

MIC 6104: COMPUTER AIDED DESIGN METHODOLOGIES AND TOOLS

Max. Marks: 50
Credit Theory : 3
Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

• Introduction to VLSI design methodologies and supporting CAD tool environment. Overview of C and Data structures, Graphics and CIF, concepts and structure and algorithms for some of the CAD tools.
• Schematic editors, layout editors, Module generators, silicon compliers, placement and routing tools.
• Behavioral, functional, logic and circuit simulators, Aids for test vector generation and testing.

References:
1. Computer Aids for VLSI by Steven M. Rubin (Addison-Wesley) 1980
3. An introduction to VLSI Physical design, Majid Serafzadeh, McGraw Hill.2002

PRACTICAL
Study of
schematic,
layout editors,
layout of gates, cells,
layout optimization,
use of silicon compliers.

MIC 6105: HARDWARE DESCRIPTION LANGUAGES AND VLSI DESIGN

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

- Design Environment, Design automation, role of EDA tools in design automation, introduction to different EDA tools, simulation and synthesis issues.
- Design entry through schematic, Design simulation with SPICE, Designing with VHDL-features and capabilities of VHDL, levels of abstraction and basic building blocks, modes and language elements, behavior modeling, Data flow and structural modeling.
- VHDL description of combinational circuits, VHDL modeling of finite state machines, PLD based system design- features of different CALD devices, physical downloading of design on CPLD chip, FPGA chip.

References:

1. VHDL by Douglas Perry, Tata Mc Graw Hill 2004
2. VHDL Analysis & Modelling of Digital system by Navabi Z., Mc Graw Hill, 2002
MIC 6106: MATERIAL SCIENCE & ENGINEERING

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

• Material Science: Atomic Bonding, Crystal structure and Defects, Diffusion, Mechanical Behaviour, Thermal Behaviour, Failure Analysis & prevention.


• Advanced Semiconductor Materials: Band structure, carrier concentration, Electrical Mechanical and optical properties of Gallium Nitride, Aluminium Nitride, Indium Nitride, Boron Nitride, Silicon Carbide, Silicon-germanium (Sil-xGex).

• Materials of special applications viz. cryogenic, high temperature, high frequency applications.

References:

MIC 6107: EMBEDDED SYSTEM DESIGN

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

• Introduction: A system, processors and other hardware units for embedded systems, embedded into system, regular processors and microcontrollers for embedded systems.
• **Hardware Aspects**: Brief discussion about processor structure, registers, memories, parallel and serial communication and ports, timers and interrupts.

• **Programming Tools and handheld Devices**: Using embedded C++, use of RTOS µc/os-I I, use of RTOS Vx Works, Kernel of an embedded system and device drivers.

• **Using Multiple Processors in Embedded Systems**: Multiple process in parallel, modeling tools for a multiprocessor system, distributed embedded systems, Systems on chip(SOC).

• **Design of an embedded system**: System design, design cycle development phase for an embedded system, users of target systems, emulator and ICE, use of software tools for embedded systems, scopes and analyzers for system hardware tests.

**References**:

1. Embedded Systems, Raj Kamal, Tata Mcgraw Hill. 2004
SECOND SEMESTER

MIC 6201: DIGITAL INTEGRATED CIRCUITS & SYSTEMS

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

- Noise Considerations in logic families.
- Digital system implementation using algorithmic state m/c concepts, Register transfer, bus clocking and control, asynchronous and synchronous systems.
- High speed adders, multipliers, FIFOs, and Barrel shifters, ALU control semiconductors for memories and PLAs, microprogrammed and PLA based control design.
- Data transfer techniques-examples of interface chips. Channel communication-protocols and standard.

References:


MIC 6202: MEASUREMENT AND CHARACTERIZATION TECHNIQUES

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

- Measurement of Resistively, Film thickness, reflectivity, refractive-index, stress, line width.
- Doping profile, Electron Beam Techniques (STM, AFM, TEM, SEM, electron beam induced current (EBIC) and voltage contrast technique).
- AES, Electron Microphone (EDX), LEED, RHEED, Ion beam Techniques (SIMS, RBS), X-ray techniques (XPS, X-ray Topography).
References:
1. Imperfections and Impurities in Semiconductor Silicon By K.V. Ravi, John Wiley and Sons.
2. Characterization of Semiconductor Materials by Philip F. Kare and Greydon B. Laubee, Mc-Graw Hill.

MIC 6203: ARCHITECTURE OF VLSI SYSTEMS

Max. Marks: 50

Credit Theory: 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

• Overview of architectural schemes, organization, representations and systems, single processor design, mechanism for higher performance.
• CISC Vs RISC, memory organization, cache Memory, I/O subsystems and control unit design, Algorithms.
• Specific architecture, upper computer architecture, pipeline and overlap processing, data flow, systolic, distributed and paralleled architectures.

References:
3. Computer system organization and Architecture, Carpinellie, Pearson Education. 2001
MIC 6204: ANALOG AND MIXED SIGNAL DEVICE DESIGN

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

PART-A

Analog VLSI issues in CMOS technologies, Basic MOS Models, SPICE Models and frequency dependent parameters, Basic NMOS/CMOS Gain stage. Single stage amplifiers:-basic concepts, common-source stage, source follower, common-gate stage.current sources and sinks. Passive and active current mirrors:-basic current mirrors, cascode current mirrors, active current mirrors. Voltage and current references.

PART-B


Textbooks :

PRACTICAL

- Simulation of analog integrated circuits
- Simulation & characterization of mixed signal devices

MIC 6205: ADVANCED MEMORY TECHNOLOGY AND DESIGN

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.
• Basics of Memory, Advanced Semiconductor Memories, Memory Device and Process Technology, Static Random Access Memory Technology.
• High –performance Dynamic random Access Memory, Non volatile memory, Radiation effects, Ferroelectric memory, Flash Memory, Future trends.
• Basic Memory Architecture and Cell Structure, Application- Specific DRAM Architectures and Design.
• Advanced Nonvolatile Memory Design and Technology, Embedded Memory Design and Applications.

References:


MIC 6206: MEMS AND MICROSYSTEMS

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

• Overview, Working principle of microsensors & microactuation

• **Elasticity**: Stress, Strain, Stress–strain Relationship, Example: Plane Stress, Strain–stress Relationship in Anisotropic Materials, Miller Indices, Example: Miller Indices of Typical Planes.

• **Bending of Microstructures**: Static Equilibrium, Free Body Diagram, Neutral Plane and Curvature, Pure Bending, Neutral Plane for a Rectangular Cross-section, Example: Cantilever with Point Force at the Tip, Moment of Inertia and Bending Moment, Example: Moment of Inertia of a Rectangular Cross-section, Beam Equation, End-loaded Cantilever, Equivalent Stiffness, Beam Equation for Point Load and Distributed Load.


• **Electrostatic Driving and Sensing**: Energy and Co-energy, Voltage Drive, Pull-in Voltage, Forces in a Parallel-plate Actuator, Electrostatic Pressure, Contact Resistance in Parallel-plate Switches, Capacitive Accelerometer.

• **Fabrication**: Introduction, Photolithography, Patterning, Lift-off, Bulk Micromachining, Angle of Walls in Silicon (100) Etching, Surface Micromachining, Example: Cantilever Fabrication by Surface Micromachining.

**References:**
2. MEMS & Microsystem- Design & Manufacture, Tai-Ran Hsu, Tata McGraw Hill.2002

**MIC 6207: RF and High Speed Digital Design**

Max. Marks: 50

Credit Theory : 3

**Note for paper setter**: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

• High speed Design: ideal transmission line fundamentals, Crosstalk.

• Non Ideal interconnect issues, connectors packages and vias, Non ideal return paths, simultaneous switching noise, and power delivery, buffer modeling, digital timing analysis, timing specific design methodologies, radiated emissions compliance and system noise minimization, high speed measurement techniques.
• RF Design: Introduction to RF Electronics, basic concepts in RF design, MOS Review, Path Loss Small Signal Model, Receiver Design RF Transceivers, Low Noise RF amplifiers and Mixers, RF Power amplifiers, RF Oscillators.

References:

THIRD SEMESTER

MIC 7101: LOW POWER DIGITAL CMOS DESIGN

Max. Marks: 50
Credit Theory : 3
Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.

- Hierarchy of limits of power.
- Sources of power consumption, power estimation, Synthesis for low power, Voltage scaling approaches.
- Design and test of low power circuits, Adiabatic switching, Minimizing switched capacitance.
- Low power static RAM architecture, Low energy computing using energy recovery techniques, low power Programmable computation, Software design for low power.

References:
1. Low power CMOS VLSI Circuit Design, Kaushik Roy and Sharat Parsad, John Wiley & Sons. 1998

MIC 7102: Microelectronics Packaging and Testing

Max. Marks: 50
Credit Theory : 3
Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.
• **Packaging:** Introduction, Packaging Hierarchy, Package parameters, packaging substrates, package types, Hermetic packages, die attachment techniques, package parasitic, package modeling, packaging in wireless application, future trends.

• **Testing:** Introduction, basic concepts, DFT, importance of test, boundary scan test, boundary scan controller, faults, faults models, physical faults, stuck-at faults, logical faults, CAD for stuck-at faults and path delays, IDQ tests, fault collapsing, fault/Automatic test pattern generation, Basic, ATPG algorithm, PODEM algorithm, Built-in self test, LPSR, MISR.

References:

**MIC 7103: NANOSCALE DEVICES AND SYSTEMS**

Max. Marks: 50

Credit Theory : 3

Note for paper setter: Total of seven questions may be set covering the whole syllabus. Candidates will be required to attempt any five.
• Introduction, sub micron scaling, ballistic effects in MOS Devices, quantum transport phenomenon, nanoscale modeling.

• Overview of Quantum Dots, Resonant tunneling devices (Diodes and transistors), Single electron effects and Coulomb Blockade, Introduction to Nano electro mechanical systems (NEMS).

• Introduction to Molecular electronic devices, self assembled monolayers (SAM), Diodes, Optoelectronic Devices, Switches, Nanowires, programmable logic arrays, digital gates, flip-flops, shift registers, memories, rectifiers, Overview of nano materials.

• Nano Fabrication Techniques (Lithography, Self-Assemble, contact imprinting and Binding of organics and semiconductors).

References:
1. Transport in Nanostructures, Ferry, David K. and Goodnick, Stephen Marshall
   Cambridge University Press.
2. Nanotechnology: G. Timp, Bell Labs, Murray Hill, NJ (Ed.)

Preliminary Thesis and Thesis

Each student will be required to work on the Preliminary Thesis and Thesis approved by department faculty that will span III and IV semesters during which periodic progress reports will be monitored. At the end of III semester, Preliminary Thesis progress will be evaluated by the departmental faculty.

At the end of IV semester, the student will submit the Thesis.