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Note:
*marks refer to mid semester evaluation and end semester evaluation.
Note: Examiner shall set eight questions, four from Part-A and four from Part-B of the syllabus. Candidate will be required to attempt any five questions selecting at least two questions from Part A and two from Part B.

Part-A
1. **Power Flow Studies**

2. **Power System Controls**
Generator-Voltage Control, Turbine-Governor Control, Load-Frequency Control (single area and two area case), Economic Dispatch, Introduction to Optimal Power Flow. 10 h

Part-B
3. **Transient Stability Studies**
Introduction of power system stability, The Swing Equation, Simplified Synchronous Machine Model and System Equivalents, Stead state stability, Transient stability, The Equal-Area Criterion for sudden change in mechanical input, sudden loss of one parallel lines, sudden short circuit on one parallel lines and effect of clearing time on stability, Numerical Integration of the Swing Equation, Design Methods for Improving Transient Stability. 18 h

4. **Facts Devices**
FACTS Technology, objectives, types of controllers, FACTS Devices: STATCOM, SSG, SVG, UPFC and SSSC. 4 h

Text Book

Other Recommended Books
EE651
Computer Aided Power Systems
Analysis Laboratory

Marks: 50  L T P
Credits : 2   0 0 3

Note: At least four design / analysis projects relating to the following.
1. Power flow analysis.
2. Power flow control
3. Economic dispatch
4. Transient stability studies.
5. Load frequency control
6. FACTS controller
EE602
Microcontroller, PLCs and Applications

Examination Details:
- External: 50
- Sessional: 50
- Credits: 4
- L T P: 3 1 0

Note: Examiner shall set eight questions, four from Part-A and four from Part-B of the syllabus. Candidate will be required to attempt any five questions selecting at least two questions from Part A and two from Part B.

Part-A
Introduction: Microcontroller, Comparison of Microprocessor and Microcontroller, microcontroller and embedded processors.
- 2 h

The 8051 Architecture: 8051 Microcontroller hardware, Input/Output Pins, Ports, and Circuits, External memory, Counter & timers, Serial Data Input/Output, Interrupts
- 6 h

8051 Assembly Language Programming: Introduction to 8051 Assembly programming, Assembling and running an 8051 program. Data Types and directives. Addressing modes and accessing memory using various addressing modes. Arithmetic instructions and programs, Logic instructions and programs, Single bit instructions and programming, Jump loop and call instructions, I/O Port programming, Timer/counter programming in the 8051
- 8 h

Serial Communication: 8051 connection to RS 232, 8051 serial communication Programming.
- 3 h

Part-B
Real World Interfacing: LCD, ADC and sensors, Stepper motor, keyboard, DAC and external memory
- 7 h

Ladder Diagram Fundamentals: Basic Components and their symbols, Fundamentals of Ladder Diagrams, Machine Control Terminology
- 4 h

Introduction to PLC: Brief History, PLC configurations, System Block Diagram, Update - solve the ladder-update
- 4 h

Fundamental PLC programming: Introduction, Physical components, Program Components, Internal Relays, Disagreement Circuit, Majority Circuit, Oscillator, Holding Contacts, Always on and always off contacts, Ladder Diagrams having more than one rung
- 6 h

Mnemonic Programming Code: AND Ladder Rung, Entering Normally closed contacts, OR Ladder Rung, Simple Branches, Complex Branches
- 5 h

Text Books
- The 8051 Microcontroller and embedded Systems by: Ali Mazidi
- Programmable Logic Controllers by John Hackworth & Frederick Hackworth

Recommended Books:
- The 8051 Microcontroller Architecture, Programming & application, by Ayala
- Programmable logic controllers Principles & applications, John W. Webb, Prentice Hall
EE-652
Micro Controller, PLCs and Applications Lab

Marks: 50          L T P
Credits : 2          0 0 3

List of Experiments:

Note: At least eight experiments to be done selecting at least two from the last experiment.

1. Study of 8051/8031 Micro controller kits.
2. Write a program to add two numbers lying at two memory locations and display the result.
3. Write a program for multiplication of two numbers lying at memory location and display the result.
4. Write a program to check a number for being ODD or EVEN and show the result on display.
5. Write a program to split a byte in two nibbles and show the two nibbles on display.
6. Write a Program to arrange 10 numbers stored in memory location in Ascending and Descending order.
7. Write a program to find a factorial of a given number.
8. Write a program of Flashing LED connected to port 1 of the Micro Controller
9. Write a program to generate a Ramp waveform using DAC with micro controller.
10. Write a program to interface the ADC.
11. Write a program to control a stepper motor in direction, speed and number of steps.

Write Ladder programs (at least two) using PLC for control of simple industrial Processes.
EE-603
Digital Signal Processing

External: 50         L T P
Sessional: 50         3 1 0
Credits : 4

Course duration: 45 lecturers of one hour duration each
Note: Examiner shall set eight questions, four from Part-A and four from Part-B of the syllabus. Candidate will be required to attempt any five questions selecting at least two questions from Part A and two from Part B.

PART A

INTRODUCTION (05)
Basic Elements of Digital Signal Processing Systems, Need and advantages of Digital Signal Processing; Classification of systems: Continuous, discrete, linear, causal, stable, dynamic, recursive, time variance; classification of signals: continuous and discrete, energy and power; Sampling Theorem, Practical sampling.

DISCRETE TIME SYSTEM ANALYSIS (07)
Linear Time Invariant systems, Stability and Causality. Solution of Linear constant coefficient difference equations, Convolution, Correlation, Z- Transform and its properties, Inverse Z transform, Solution of difference equation using Z-Transform.

FREQUENCY DOMAIN REPRESENTATION OF SIGNALS & SYSTEMS (10)
Fourier series & Fourier Transform of Discrete time signals, Discrete Fourier Transform and its properties, Fast Fourier Transform, Decimation in time and Decimation in frequency algorithms. Frequency domain representation of discrete time systems.

PART B

DESIGN OF DIGITAL FILTERS (10)
Fundamentals of filter design, Design of FIR Filters: Window technique, Frequency sampling technique IIR Filters: Analog filter approximations - Butterworth, Chebyshev and Elliptic filter, Design of IIR Digital filters from analog filters, IIR Filter Design by Impulse Invariance &Bilinear Transformation, Frequency transformation in analog and digital domain

IMPLEMENTATION OF DISCRETE TIME SYSTEMS (05)
Block diagrams and signal flow graphs for FIR and IIR systems. Direct form, Cascade and Frequency Sampling Structures for FIR systems, Direct forms, Cascade and Parallel form realization of IIR systems, Finite Word Length Effects.

DSP PROCESSORS (08)
Introduction to fixed point and floating point processors and their architecture, TMS320C5X Architecture, Memory, Addressing Modes.

Recommended Books:
2. “Digital Signal Processing” by E C Ifeacher and B W Jervis

EE-653
Digital Signal Processing Lab

Marks: 50
Credits : 2
L T P 0 0 3

List of Experiments:

Note: At least eight experiments to be done .

1. Generating & Plotting Discrete time signals using MATLAB.
2. Use of basic multi-signal processing signals of MATLAB
3. To perform different operations -addition, multiplication, scaling, folding, and shifting using MATLAB.
4. Convolution of Causal & Non Causal sequences in MATLAB.
5. Auto & Cross-Correlation in MATLAB.
7. DFT & IDFT of two sequences.
8. FFT of two Sequences.
9. FIR Filter Design using Window Method in MATLAB.
10. IIR Filter Design using Bilinear Transformation in MATLAB.
11. IIR Filter Design using Impulse Invariance in MATLAB.
12. Butterworth and Chebyshev Digital IIR Filters in MATLAB.
13. Implementation of Filter Structures in MATLAB.
15. System Design based on DSP kits.
EE- 604
ELECTRONIC SYSTEMS DESIGN

External: 50         L T P
Sessional: 50         3 1 0
Credits : 4

Note: Examiner shall set eight questions, four from Part-A and four from Part-B of the syllabus. Candidate will be required to attempt any five questions selecting at least two questions from Part A and two from Part B.

Part-A

COMBINATIONAL CIRCUITS (15)

Error Correction and Detection: Error detection and correction techniques, Single error detection, Single error correction with double error

VHDL models and simulation of combinational circuits such as Multiplexers, Encoders, Decoders, Code converters, Comparators, Implementation of Boolean functions etc.

PART-B

FAULTS (05)
Fault detection and Location in combinational circuits: Different methods of detecting and locating Faults in combinational circuits.

SEQUENTIAL CIRCUITS (15)
VHDL Models and simulation of sequential circuits, Shift registers, Counters etc.

FAULTS (05)
Fault detection and Location in sequential circuits.

TEXT BOOKS
Digital circuits and Logic Design By Lee
Switching and Finite Automata Theory, Kohavi
A VHDL Primer, Bhasker; Prentice Hall

OTHER RECOMMENDED BOOKS
Computer Logic Design, Morris Mano
Switching circuits for Engineers, Marcus
Introduction to Digital systems, James Palmier, David Perlman
Digital System Design using VHDL, Charles. H. Roth; PWS
VHDL-IV Edition:Perry; TMH
Fundamentals of Digital Logic with VHDL Design: Brown and Vranesic; TMH
EE -654
ELECTRONIC SYSTEMS DESIGN LAB

Marks: 50 L T P
Credits : 2 0 0 3

Note: At least eight experiments are to be performed.

List of Experiments:

1. To Design and test the minimized circuit of Full Adder.
2. To Design and test the minimized circuit of BCD to Binary Converter
3. Implement decade counter using minimum number of gates
4. To test the minimized circuit of Decimal to BCD Encoder
5. Design and test hexadecimal to binary Encoder
6. Implement and test BCD TO 7-Segment decoder
7. Design a sequence detector to detect a given sequence
8. Design and test twisted type ring counter
9. Implement the minimized circuit of Modulo-6 counter
10. To design, implement and test a 16 :4 multiplexer using logic gates.
11. To design, implement and test a 4:16 demultiplexer using logic gates.
12. Design & test Johnson Counter.
EE605
COMPUTER NETWORKS

External: 50         L T P
Sessional: 50         3 1 0
Credits : 4

Note: Examiner shall set eight questions, four from Part-A and four from Part-B of the syllabus. Candidate will be required to attempt any five questions selecting at least two questions from Part A and two from Part B.

Part-A

Introduction (6)
Data Transmission concepts; switching; Modulation; multiplexing; Network Hardware: LAN, MAN, WAN, Wireless Networks, Internet works; Network Software: Layer, Protocols, interfaces and services; Reference Model: OSI, TCP/IP and their comparison.

Physical Layer (10)

Data Link Layer (10)
Framing; Error control; Error Correction & Error Detection; Sliding window protocols; Examples of DLL Protocols – HDLC,SLIP, PPP ; Medium Access Sub Layer: Channel Allocation, MAC protocols – ALOHA,CSMA protocols, Collision free protocols, Limited Contention Protocols, Wireless Protocols, IEEE 802.3,802.4,802.5 standards and their comparison. Bridges: Transparent, source routing, remote.

Part-B

Network Layer (8)
Design issues, routing algorithms (shortest path, flooding, flow based, distance vector, hierarchical, broadcast, multicast, for mobile host). Introduction to Congestion control algorithms.

Transport Layer (5)
Addressing, establishing and releasing connection, flow control & buffering, multiplexing, crash recovery, Internet Transport protocol (TCP and UDP).

Application Layer (6)
Basics of Network security, Domain Name System, Introduction of Simple Network Management Protocol, Electronic mail and FTP.

Text Books
1. Computer Networks Andrew S. Tanenbaum (PHI)
2. Data Communications and Networking, 3/e Behrouz A Forouzan (Mcgraw-hill)

Other Recommended Books
1. Data and Communication William Stallings (PHI)
2. Data & Computer Communication Douglos E. Coomer (Addison Wessl)