PANJAB UNIVERSITY, CHANDIGARH-160014 (INDIA)
(Estd. under the Panjab University Act VII of 1947 - enacted by the Govt. of India)

FACULTY OF ENGINEERING & TECHNOLOGY

SYLLABI

AND THE

REGULATIONS

FOR

Bachelor of Engineering (Electronics & Communication)
Third-Eighth Semesters
Examinations, 2011-2012

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## Scheme of Examination of B.E.

### Third Semester

<table>
<thead>
<tr>
<th>Theory Paper Code</th>
<th>Paper Title</th>
<th>Hours/Week L+T</th>
<th>Credit Theory</th>
<th>Marks Uni. Exam</th>
<th>Int. Ass.</th>
<th>Hours/Week</th>
<th>Credit Practical</th>
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<tr>
<td>EC306</td>
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Grand Total: 800  19  19  300  300  8  4  200  
Total Credit : 23

### Fourth Semester

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Total Credit : 27
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Eighth Semester

### OPTION -1

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### OPTION - 2

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#### Elective – I

- EC704: Embedded System Design
- EC705: Advanced Digital Communication
- EC706: Radar Engineering
- EC707: Web Technologies

#### Elective – II

- EC804: Neural Networks & Fuzzy Logic
- EC805: Artificial Intelligence
- EC806: Digital Image Processing
- EC807: Nano Technology

### OR OPTION 2

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<td>Industrial training</td>
<td>6 Months</td>
<td>650</td>
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Student can exercise option 1 or option 2 according to the following:

A student may opt for one semester training in live of subject of 8th semester. The marks for six months training will be equal to the total marks of 8th semester study. A student can opt for six months semester training under following conditions:

a. The student got selected for the job in campus placement and the employer is willing to take that student for the training.

b. The student got offer of pursuing training from reputed government research organization/ govt. sponsored project/govt. research institution provided that student should not be paying any money to get trained. For pursuing this training student need the prior approval from the chairperson/Coordinator of the respective department/branch.
THIRD SEMESTER

Paper Title: Semiconductor Electronics (Theory)

Paper Code: EC 306 Max. Marks/ Credit: 50/3 Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Transistor characteristics : [10]
Junction transistor, transistor current components, current gain, transistor as an amplifier, common emitter, common base, common collector configurations, Input & output characteristics in CE, CB & CC configurations, photo transistor & its characteristics, unijunction transistor & its characteristics.

Transistor at low frequencies: [08]
Graphical analysis of CE configuration two port devices and hybrid model, h-parameters, Comparison of amplifier configurations of circuits

Transistor biasing and Thermal stabilization: [08]
Concept of biasing & biasing of BJT circuits, Operating point, bias stability, stabilization against variation in Ico, Vbe, and β, thermal run away, thermal stability.

PART B

Field Effect Transistor: [09]
Junction field effect transistor, JFET characteristics, pinch off voltage and equivalent circuit, MOSFETs - their modes of operation and characteristics, equivalent circuit, biasing of FETs.

Power amplifiers: [10]
Classification of amplifiers, Class A large signal amplifier, second and higher harmonic distortion, transformer coupled amplifiers, Efficiency of amplifiers, Push pull amplifiers (class A & class B).

Recommended Books:

1. Integrated Electronics, Millman & Halkias (Mc-Graw Hill)
2. Microelectronics Circuits, AS Sedra & KC Smith (OXFORD)
3. Electronics Devices & Circuit Theory, RL Boylestead & L Nashelsky (PHI)
4. Electronic Circuit Analysis & Design, Donald A. Neamen (TMH)

Paper Title:- Semiconductor Electronics(Practical)
List of Experiments

1. To study the specification sheet & draw the characteristics of transistor in CB or CE configuration.
2. To study the specification sheet & draw the characteristics of FET in CD or CC configuration.
3. To draw the frequency response of a single stage BJT amplifier.
4. To measure the voltage and current gain of a BJT amplifier.
5. To measure the distortion in the output of a push pull amplifier.

To simulate the following using P-spice

1. Frequency Response of a single state FET amplifier.
2. Voltage and current gain of BJT amplifier.
3. Distortion of a push pull power amplifier.
Recommended Books:

3. Antennas and Wave Propagation by G S N Raju, Pearson publications, Edition 1ST

Paper Title: FILTERS AND TRANSMISSION LINES (THEORY)

Paper Code: EC 308             Max. Marks/ Credit: 50/3             Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Impedance Functions and Networks functions:
Concept of complex frequency, Transform Impedance and transform circuits, Network functions for the one port and two port, Calculation of network functions, Poles and Zeros for Network functions, Restrictions on Poles and Zeros, Locations for Driving Point and Transfer functions, Time domain behavior from Pole and Zero plot, Stability of Active networks. [09]

Filter Synthesis:
Classification of filters, Characteristics, impedance (input & characteristic) and propagation constant of pure reactive network, Ladder Network, T-section, Π-section, Pass and stop bands, Constant –K low pass and high pass filters, m-derived T and Π- section, Design of k and m-derived filters, Band pass filters, band elimination filters, Composite filters. [12]

PART B

Two Port Parameters:
Relationship of Two port variables, Short Circuit Admittance and Open circuit Impedance parameters, Transmission and hybrid parameters. [06]

Sinusoidal Steady State Analysis:
Network Synthesis for two terminal network, Foster and Cauer forms. [03]

Transmission Lines:
Line parameters, Inductance and capacitance of a line of two parallel conductors, inductance of coaxial line, Line of Cascaded T-section, Transmission line-general solution, Physical significance of the equations, the infinite line, wavelength, velocity of propagation, waveform distortion, distortionless line, telephone cable, Reflection on a line not terminated in $Z_0$, Reflection constant, Line calculation, Input and transfer impedance, open and short circuited lines, Reflection factor and reflection loss, parameters of open wire line and coaxial line at high frequencies, constants for the line of zero dissipation, Voltage and currents on
dissipationless line, standing wave nodes, standing wave ratio. Input impedance of dissipationless line, power loss in unmatched lines, single stub matching and smithchart.

**Recommended Books**

7. Network Analysis by M.E. Van Valkenburg (PHI), Edition 3+0RD.

**Paper Title:- FILTERS AND TRANSMISSION LINES (PRACTICAL)**

**Paper Code: EC358**

Max. Marks : 25 Credit: 1

**List of Experiments**

1. To Design & implement a constant K low pass / high pass filter.
2. To Design & implement a band pass filter.
3. To Design & implement a m-derived low pass / high pass filter
4. To Design & implement a composite low pass/ high pass filter.
5. To Measure the characteristics and attenuation of a Transmission line.
6. To Measure the input impedance of a Transmission line.
7. To Measure phase displacement between the current and voltage at input of Transmission line.
8. To Study the Frequency characteristics and stationary waves of a Transmission line.
9. To Measure Signal Phase shift along the line.
10. Fault localization within the line.

**Paper Title:- Digital Electronics (Theory)**

**Paper Code: EC 309**

Max. Marks/ Credit: 50/3 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**

**Introduction**

Concept of digitisation, Representation of Logic, Logic Variables, Boolean Algebra, Boolean Expressions and minimization of Boolean expression using K-Map (up to five variables), Review of Logic Gates, design & Implementation of Adder, Subtractor, Multiplexer, DeMultiplexer, Encoder, Decoder, ROM, Digital Comparators, Code Converters using gate, multiplexers / decoders

**Flip-Flops**
A 1-bit memory cell, clocked & unclocked flip flop, S-R Flip-Flop, JK Flip-Flop, Race around Condition, Master Slave Flip-Flop, D&T type Flip-Flop

Counters & Shift Registers
Ripple Counters, Design of Modulo-N ripple counter, Presettable Counters, Up-Down counter, design of synchronous counters with and without lockout conditions, design of shift registers with shift-left, shift-right & parallel load facilities, Universal shift Registers

PART B

Data Converters
Sample & Hold switch, D/A converters: weighted resistor type, R-2R Ladder type; A/D Converters: Counter-Ramp type, Dual Slope Type, Successive approximation type, flash type; Specifications of ADC & DAC

Digital Logic families
Characteristics of digital circuits: fan in, fan-out, power dissipation, propagation delay, noise margin; Transistor-transistor Logic (TTL), manufacturer Data Sheets & Specifications, Types of TTL Gates (Schottky, standard, low power, high speed). Emitter Coupled Logic (ECL), Manufacturers Data sheets & Specifications, Comparison of Characteristics of TTL and ECL, Tristate Logic & its applications.

Semiconductor Memories & Programmable Logic
ROM, PROM, EPROM, EEPROM; RAM: Static RAM, Typical Memory Cell, Memory Organisation, Dynamic RAM cell, Reading, & Writing Operation in RAM, PLA, PAL & FPGA

Recommended Books
2. Integrated Electronics by Millman & Halkias, TMH
3. Digital System Principles & Applications by R J Tocci (PHI)

Paper Title: Digital Electronics (Practical)

Paper Code: EC359 Max. Marks: 25 Credit: 1

List of Experiments
1. To Study the data sheets of TTL and ECL gates
2. Verify the truth tables of various gates, RS, D, JK Flip Flops
3. To design and implement a Modulo-N Counter
4. To Design and implement a Universal shift register
5. To Perform arithmetic & Logic operations on two 4-bit binary numbers using an ALU.
6. To Transfer the Data between Three Registers through Tristate Circuit
7. To Understand Decoder/Driver and their applications with display. To display a count from 00 to 99 with a delay of N seconds.
8. Design & Implementation of synchronous counter
10. To convert 8 bit Digital data to Analog value using DAC
11. To convert Analog value into 8 bit Digital data using ADC

Paper Title: Engineering Mathematics – III

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**Part - A**

Sequences and Series: (08)

Linear Algebra: (07)
Concept of linear independence and dependence, Rank of a matrix: Row – Echelon form, System of linear equations: Condition for consistency of system of linear equations, Solution by Gauss elimination method. Inverse of a matrix: Gauss – Jordan elimination method (Scope as in Chapter 6, Sections 6.3 – 6.5, 6.7 of Reference 1).
Eigen values, eigen vectors, Cayley – Hamilton theorem (statement only). Similarity of matrices, Basis of eigenvectors, diagonalization (Scope as in Chapter 7, Sections 7.1, 7.5 of Reference 1).

**Part - B**

Complex Functions: (08)
Definition of a Complex Function, Concept of continuity and differentiability of a complex function, Cauchy – Riemann equations, necessary and sufficient conditions for differentiability (Statement only). Study of complex functions: Exponential function, Trigonometric functions, Hyperbolic functions, real and imaginary part of trigonometric and hyperbolic functions, Logarithmic functions of a complex variable, complex exponents (Scope as in Chapter 12, Sections 12.3 – 12.4, 12.6 – 12.8 of Reference 1).

Laurent Series of function of complex variable, Singularities and Zeros, Residues at simple poles and Residue at a pole of any order, Residue Theorem (Statement only) and its simple applications (Scope as in Chapter 15, Sections 15.1 – 15.3 of Reference 1). (07)
Conformal Mappings, Linear Fractional Transformations (Scope as in Chapter 12, Sections 12.5, 12.9 of Reference 1). (08)

References:

Paper Title:- Object Oriented Programming (Theory)

Paper Code: EC 310  Max. Marks/ Credit: 50/3  Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**
Principles Of Objected Oriented Programming
Advantages of OOP, comparison of OOP with Procedural Paradigm [3]

C++ Constructs
Tokens, Expressions and control structures, various data types, and data structures, Variable declarations,
Dynamic Initializations, Operators and Scope of Operators, Typecasting, Unformatted and formatted console
I/O Operations [3]

Functions
Classes and Objects: Prototyping, Referencing the variables in functions, Inline, static and friend functions.
Memory allocation for classes and objects. Arrays of objects, pointers to member functions. [5]

Constructors and Destructors
Characteristics and its various types, Dynamic Constructors, Applications, Order of Invocation, C++
garbage collection, dynamic memory allocation. [5]

Polymorphism
Using function and Operator overloading, overloading using friend Functions, type conversions from basic
data types to user defined and vice versa. [5]

PART B

Inheritance [6]
Derived classes, types of inheritance, various types of classes, Invocation of Constructors and Destructors in
Inheritance, aggregation, composition, classification hierarchies, metaclass/abstract classes.

Pointers
constant pointers, Use of this Pointer, Pointer to derived and base classes, virtual functions, Bindings, Pure
virtual Functions and polymorphism [5]

I/O Operations and Files
Classes for files, Operations on a file, file pointers [4]

Generic Programming with Templates [6]
Definition of class template, Function Templates, Overloading Template Functions, Class templates
and member functions templates with parameters, Standard C++ classes, persistent objects, streams
and files, namespaces, exception handling, generic classes, standard template library: Library
organization and containers, standard containers, algorithm and Function objects, iterators and
allocators, strings, streams, manipulators, user defined manipulators and vectors

Introduction
Object Oriented System, Analysis and Design [3]

Recommended Books
1. Object Oriented Programming with C++ By Bala Guruswamy, TMH, Edition 3rd
3. The C++ Programming Language By Bjarne Stroutstrup, Edition 3rd
5. The Complete Reference to c++ By Schildt, TMH, Edition 4th

Paper Title: Object Oriented Programming (Practical)

Paper Code: EC 360 Max. Marks: 25 Credit: 1

List of Experiments

1. Implementation of Functions, Classes and Objects
2. Constructors and Destructors
3. Operator Overloading and Type Conversion
4. Inheritance and Virtual Functions
5. Files
6. Exception Handling and Generic Programming

FOURTH SEMESTER

Paper Title: Communication Theory

Paper Code: EC 407 Max. Marks/ Credit: 50/4 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Signal & its Representations

Random Signal Theory
Sample space, random variables-discrete & Continuous, examples of probability Density Functions- Moments, joint & conditional PDF density functions of sums, Transformation, concept of correlation, auto & Cross-correlation functions, white Noise. [8]

Transmission of Signals through Networks
PART B

Noise & Interference
Classification of Noise, Sources of noises, atmospheric shots, Thermal noise, noise in Semiconductors, Noise spectral density, Noise calculations, Noise Figures of devices & circuits, cascaded networks, Minimum noise, Figures of networks. Experimental determination of Noise Factor

[07]

Basic Information Theory
Concept Information, Entropies of Discrete Systems, Rate of transmission- Redundancy, Efficiency & Channel capacity, Source encoding including Huffman’s Technique, continuous Channel- Entropy maximization, Transmission rate of Channels, capacity of Noisy channels. Discussion of Shannon’s Coding theorem, Comparison of Analog & Digital Communication Systems with reference to the Ideal Channel Capacity Theorem.

[14]

Recommended Books
Introduction to Modern Communication by P D Sharma, Edition Latest
Introduction to Information Theory by F M Reza, Edition Latest

Paper Title: - Analog Electronic Circuits (Theory)

Paper Code: EC 408 Max. Marks/ Credit: 50/4 Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Response of transistor Amplifier
Review Biasing, classification of amplifier, distortion in amplifiers, frequency & phase response of an amplifier, RC coupled amplifier, its low and high frequency responses, transistor model at high frequencies for CE and Emitter follower configuration, high frequency response of two cascaded CE transistor stages

[9]

Feedback and Stability
Introduction to feedback, Basic-Feedback Concepts, Ideal Feedback Topologies, Voltage(Series-Shunt) Amplifiers, Current(Series-Shunt) Amplifiers, Transconductance(Series-Series) Amplifiers, Transresistance(Shunt-Shunt) Amplifiers,

Operational Amplifier
[10]
Differential Amplifier, Block diagram representation of a typical Op-amp, Interpreting of a typical set of data sheets, ideal op-amp, equivalent circuit. of op-amp, ideal voltage transfer curve, open loop op-amp configuration, the practical op-amp, input offset voltage, input bias current, input offset current, total output offset voltage, thermal drift, noise, common mode configuration, CMRR,. Frequency Response, Frequency response of internally compensated Op-Amps, Frequency response of Non-compensated OP-Amps, Open loop voltage gain as a function of frequency, Closed loop frequency response, Slew rate

PART B

Op-amp Applications
DC and AC Amplifiers, summing, Voltage-to-current converter, current to voltage converter, the Integrator, the Differentiator, Comparator, Zero-crossing detector, Voltage to frequency and frequency to voltage
converters, Clippers and Clampers, Sample and Hold Circuit, Instrumentation Amplifier.

10

Active Filter, Oscillators & Tuned Amplifiers
Active filters, Essentials of Oscillator, Types of Oscillator, Sinusoidal Oscillator, Schmitt Trigger Circuits, Introduction of Tuned Amplifiers, Single & Double Tuned Amplifiers

Recommended Books

1. Electronics Circuit Analysis and Design by Donald A. Neamen, Tata McGraw Hill
3. Integrated electronics by Millman & Halkias, TMH, Latest Edition

Paper Title: Analog Electronic Circuits (Practical)

Paper Code: EC 458 Max. Marks: 50/Credit: 1
List of Experiments

1. To study the Pspice Simulation software
2. Design fabrication & testing of Differentiator Circuits using Op-Amp & simulate using P-spice
3. Design fabrication & testing of Integrator Circuits using Op-Amp & simulate using P-spice
4. Design fabrication & testing of adder/Subtractor Circuits using Op-Amp & simulate using P-spice
5. Design fabrication & testing of Clippers and Clampers Circuits using Op-Amp & simulate using P-spice
6. Design fabrication & testing of Universal Active filter & simulate using P-spice
7. To study the frequency response of OP-Amp & simulate using P-spice
8. To design Butter worth Low pass filter & simulate using P-spice
9. To design Butter worth High pass filter & simulate using P-spice
10. To design Butter worth Band pass filter & simulate using P-spice
11. To design Monostable & Free running Multivibrator using 555

Paper Title: Microprocessors (Theory)

Paper Code: EC 409 Max. Marks/ Credit: 50/4 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Microprocessor Architecture and Microcomputer Systems;

Interfacing I/O Devices:

Programming the 8085:
Introduction to 8085 Assembly Language Programming, The 8085 Programming Model, Instruction Classification, Instruction Format, Data Transfer (Copy) Operations, Arithmetic Operations, Logic Operations, Branch Operations, Writing Assembly Language Programs. [8]
Programming Techniques with Additional Instructions:

PART B

Counters and Time Delays:
Counters and Time Delays, Hexadecimal Counter, Modulo Ten Counter, Generating Pulse Waveforms, Debugging Counter and Time-Delay Programs. [4]

Stack and Subroutines: Stack, Subroutine, Conditional Call and Return Instructions. [3]

Interrupts: The 8085 Interrupt, 8085 Vectored interrupts. [3]

Interfacing Data Converters:

General-Purpose Programmable Peripheral Devices:
The 8255A Programmable Peripheral Interface, Illustration: Interfacing Keyboard and Seven-Segment Display, Illustration: Bidirectional Data Transfer between Two Microcomputers, The 8254 Programmable Interval Timer, The 8259A Programmable Interrupt Controller, Direct Memory Access (DMA) and the 8257 DMA Controller, Programmable communications interface 8251. [8]

Recommended Books


Paper Title: Microprocessors (Practical)

Paper Code: EC 459 Max. Marks: 50 Credit: 1

List of Experiments

1. Familiarization of 8085 kits.
2. Verification of arithmetic and logic operations using above kits. (At least 5 programs)
3. Development of interfacing circuits of various control applications based on 8085.
4. Application of assembly language using 8085 instructions set to develop various programs.
5. Applications of data movement instructions to develop relevant programs.

Paper Title: Communication Engineering (Theory)

Paper Code: EC 410 Max. Marks/ Credit: 50/4 Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.
PART A

Amplitude Modulation & Demodulation and Systems

Frequency Modulation
Principles and generation of FM and PM signals, Reactance Modulator method, Armstrong Method, noise consideration in FM and PM system. [7]

PART B

Frequency Demodulation and FM Systems
Detection of FM and PM signals, Foster Discriminator, ratio and PLL detectors, FM Transmitter(Block Diagram), FM receiver (Block Diagram), Pre-emphasis and de-emphasis circuit. [8]

Pulse Modulation & Demodulation
Principles, generation and detection of PAM, PWM, PPM & PCM signals, noise in pulse modulation system, band width consideration, companding, delta modulation, adaptive delta modulation systems. TDM & FDM [15]

Recommended Books

1. Electronic Principles by Dennis Raddy & John Coolin, PHI, Edition Latest

Paper Title:- Communication Engineering (Practical)

Paper Code: EC 460 Max. Marks: 50 Credit : 1

List of experiments

1. To measure the modulation index of AM signals using the trapezoidal method
2. To study DSB/ SC AM signal and its demodulation using product Detector Circuit.
3. To study the voltages and waveforms of various stages of super-heterodyne receiver
4. To measure the sensitivity and selectivity of a super heterodyne radio receiver
5. To study the voltages and waveforms of various stages of FM Receiver
6. To study the pulse code modulation and de-modulation circuit
7. To study the Time division multiplexing and demultiplexing circuit
8. To study delta modulation and demodulation circuits.
9. To study sigma delta modulation and demodulation circuits.

Paper title: Operating Systems Max. Marks/ Credit: 50/4
Paper Code: EC411

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Concept of an operating systems, batch system, Multi-programmed, Time sharing, Personal Computer System, Parallel system, Real time system, General system Architecture.


Memory Management: [6]
Logical and physical address space, storage allocation and management techniques, swapping, concepts of multi programming, paging, segmentation, virtual storage management strategies, Demand Paging, Page Replacement Algorithms, Thrashing.

PART B

Information Management: [6]
File concept, Access method, Directory structure, Protection File system structure, Allocation methods, Free space management, Directory implementation, Disk structure, Disk Scheduling, Disk management, Swap space management.

Distributed-System Structures: [6]
Network operating system, Distributed operating systems, Remote services, Robustness, Design Issues.

Distributed file systems and Distributed Coordination: [6]

Case Studies: [5]
Unix O.S. Architecture, Operating system services, user perspective, representation of files in Unix system processes and their structure, Input-output system, Memory management, Unix shell, history and evolution of Unix system.

Recommended Books


Reference Books

Paper Title: Data Structures and Algorithms (Theory)

Paper Code: EC 412  Max. Marks/ Credit: 50/4  Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Introduction: Introduction to data structures; Introduction to Algorithms Complexity;

Arrays, Stacks & Queues: Concepts; Basic operations & their algorithms: Transverse, Insert, Delete, Sorting of data in these data structures; Prefix, Infix, Postfix Notations;

Lists: Concepts of Link List and their representation; Two way lists; Circular link list; Basic operations & their algorithms: Transverse, Insert, Delete, Searching and Sorting of data in List; Storage Allocation & Garbage Collection; Linked stack and queues; Generalized List; sparse matrix representation using generalized list structure;

PART B

Trees:
Binary Trees and their representation using arrays and linked lists; Trees and their applications; Binary tree transversal; Inserting, deleting and searching in binary trees; Heap & Heap Sort; General Trees; Thread binary tree; Height balance Tree (AVL); B-Tree;

Graphs and their applications:
Graphs; Linked Representation of Graphs; Graph Traversal and spanning forests; Depth first search; Breadth first search;

Sorting & Searching:
Insertion sort; Selection sort; Merging; Merge sort; Radix sort; Sequential & Binary Search; Indexed Search; Hashing schemes; Binary search Tree;

Recommended Books

2. Theory and problems of Data Structures Seymour Lipschutz (McGraw Hill), Edition 1st
FIFTH SEMESTER

Paper Title: Cyber Laws & IPR

Paper Code: ASC 506

Max Marks: 75

Time : 3Hrs

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Basics of Computer & Internet Technology [8]

Internet, ISP & domain name; Network Security; Encryption Techniques and Algorithms; Digital Signatures

Introduction to Cyber World [2]

Introduction to Cyberspace and Cyber Law; Different Components of cyber Laws; Cyber Law and Netizens

E-Commerce [7]

Introduction to E-Commerce; Different E-Commerce Models; E-Commerce Trends and Prospects; E-Commerce and Taxation; Legal Aspects of E-Commerce.

PART B

Intellectual Property Rights [12]

What are IPR, Copyright and Patents; International Treaties and Conventions; Business Software Patents; Domain Name Disputes and Resolution.

IT Act, 2000 [12]

Reasons, Aims, Objectives and Applications. Regulators under IT Act, Role of Certifying Authority; Digital Signature Certificates, Duties of the Subscribers, Cyber Crimes-Offences and Contraventions; Grey Areas of IT Act

Project Work [04]

Candidates will be required to work on a project. At the end of the course students will make a presentation and submit the project report.

Recommended Books


Paper Title: Integrated Circuits (Theory)
Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Introduction:
General classification of Integrated Circuits, advantages of ICs over Discrete Components, Computer Generations.

Thick Film and Thin Film Hybrid ICs:
Features of Hybrid IC technology, Thick Film technology, Thick film processing, Thick Film design, guidelines and applications of thick film hybrids. Thin film technology, Thin film processing, Thin film design, guidelines, advantage and applications of Thin film hybrids.

Monolithic IC Processes:

PART B

Monolithic Components:

Basic Building Blocks for ICs:
Bipolar Transistor current sources. FET current sources independent of supply voltage variations.

Recommended Books

1. Integrated circuits by K.R. Botkar, Khanna Publishers
3. VLSI Technology by Simon Sze, Tata Mc Grawhill

Paper Title: Integrated Circuits (Practical)

Paper Code: EC552 Max. Marks 50
List of Experiments

1. VI Characteristics of NMOS Transistor
2. VI Characteristics of PMOS Transistor
3. Voltage Transfer characteristics of CMOS Inverter for Inverter threshold to be Vdd/2, \( Id=1\mu A \)
4. Study the Transient characteristics of CMOS Inverter for different frequencies.
5. Design of CMOS Nand Gate
6. Design of CMOS NOR Gate
7. Design of CMOS 2:1 Mux
8. Study the characteristics of CMOS Transmission Gate
9. Study the characteristics of NMOS Pass transistor
10. Design of CMOS current source, current = 1\u00b5A
11. Design of CMOS Differential amplifier

Paper Title: Microcontrollers and Interfacing (Theory)

Paper Code: EC503 Max. Marks 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Microprocessor and Microcontroller [2]
Comparison of Microprocessor and Microcontroller, Overview of 4 bit, 8 bit, 16 bit and 32 bit Microcontrollers, Overview of 8051 family

The 8051 Architecture [12]
8051 Oscillator and clock, Program counter and Data pointer, A and B CPU registers, Flags and Process Status Word, Internal Memory and RAM, The Stack and Stack Pointer, Special Function registers, Internal ROM, Input/output pins and ports, External Memory connection, Counters and Timers, Timer Counter Interrupts, Timer Modes of operation, Serial data Interrupts and Modes, Timer flag Interrupt, Serial port Interrupt, External Interrupts, Reset, Interrupt Control, Interrupt Priority, Interrupt Destination, Software generated Interrupts.

8051 Assembly Language Programming [12]
8051 Assembly Language Mnemonics and Syntax, Data Moving Instructions, Byte Level and Bit Level Logical Operations, Rotate and Swap operations, Arithmetic Operations, Jump and Call Instructions, Calls and Subroutines, Interrupts and returns.

PART B

8051 Microcontroller Design [10]
Microcontroller Specification, A Microcontroller design, External memory and Memory Space decoding, reset and clock circuits, expanding I/O, Memory mapped I/O, Memory Address Decoding, Testing the design- Crystal test, ROM test, RAM test, Timing subroutines- Hardware and Software time delays, Lookup tables for 8051, 8051 Serial Communication, 8051 connection to RS 232, Interrupt Programming, Interrupt Priority in 8051, Programming Timer Interrupts, External hardware Interrupts and Serial Communication Interrupts.
**Real World Interfacing**

Interfacing of 8051 to LCD, ADC, DAC, Sensors, Stepper Motor, Keyboard, Interfacing to External Memory, Interfacing to the 8255.

**Recommended Books**

Sanjay Attri, “Microcontrollers and PLC’s”, Dhanpat Rai and Sons.

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**Paper Title: Microcontrollers and Interfacing (Practical)**

**Paper Code: EC553**  
Max. Marks 50

**List of Experiments**

1. Write programs for Data Moving Instructions, Byte Level and Bit Level Logical Operations, Rotate and Swap operations, Arithmetic Operations, Jump and Call Instructions, Calls and Subroutines, Interrupts and returns as follows:
   a. Write a program to compute sum of N natural numbers.
   b. Write a program to find the smallest element of an array of N integers.
   c. Write a program to perform BINARY SEARCH on an array that is sorted in ascending order.
   d. Write a program to compute the sum of odd elements of an array of 8-bit integers.
   e. Compute the address of the elements of 5 x 5 matrix
   f. Multiply two 2 x 2 matrices. Try to make it generalized.
   g. Write programs for Timer Interrupts, Serial port Interrupts
2. Write programs for Interfacing of 8051 to LCD, ADC, DAC, Sensors, Stepper Motor, keyboard, Interfacing to External Memory, Interfacing to the 8255.

**Paper title: Digital Communication (Theory)**

**Paper Code: EC504**  
Max. Marks: 100  
Time: 3 hours

**Course duration**: 45 lectures of one hour duration each

**Note for paper setter**: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**

**Signal Space Analysis**: Geometric Representation of Signals, Gram-Schmidt Orthogonalization Procedure.
**Digital modulation techniques:** PSK, FSK, MSK, QAM. Error calculations for PSK, FSK, MSK, QAM, Shannon’s limit, Signal to Noise Ratio Calculations in PCM and DM systems. [8]

**Information theory and coding:** Entropy, Capacity of a Gaussian Channel. Block codes, Convolution coding and decoding, Soft and Hard decision decoding, State & Trellis diagrams, Viterbi Algorithm, Trellis decoded modulation. [10]

**PART B**

**Multiplexing and Multiple Access:** Allocation of communication Resources, FDM/FDMA, TDM/TDMA, CDMA, SDMA, Multiple Access Communications and Architecture, Access Algorithms. [8]

**Spread Spectrum Techniques:** Spread Spectrum Overview, Pseudonoise Sequences, Direct Sequence and Frequency Hopped Systems, Synchronization of DS and FH systems, Jamming Considerations, Commercial Applications [8]

**Signal design for band-limited channels for No Inter Symbol Interference:** Pulse shaping to Reduce ISI, types of error-performance degradation, demodulation/detection of shaped pulses [7]

**Recommended Books**

1. Digital Communications by Bernard Sklar, PHI

**Paper title: Digital Communication (Practical)**

**Paper Code:** EC554 Max. Marks: 50

**List of Experiments**

1. Design and practical implementation of ASK systems
2. Design and practical implementation of PSK systems
3. Design and practical implementation of QPSK systems
4. Design and practical implementation of FSK systems
5. To study the application of CDMA in voice communications
6. To practically compare the noise in PCM and DM systems
7. To practically study Frequency Division Multiplexing.
8. To practically study Time Division Multiplexing.
9. Implementation of Viterbi algorithm using C-language

**Paper Title: Antennas and Wave Propagation (Theory)**

**Paper Code:** EC505 Max. Marks: 100 Time: 3 hours

**Course duration:** 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Antenna Radiation
Antenna Parameters: Antenna impedance, Directional patterns, Effective length, Radiation Intensity, Directivity, Power gain, Efficiency, Effective area, Equivalent circuit, Front to back ratio, polarisation and antenna temperature, Radiation field, Radiation power, Radiation resistance, Directivity and gain of an alternating current element, half wave dipole and quarter wave monopole. Effect of earth on patterns.

Antenna arrays

PART B

Practical Antennas
Top loading and tuning, rhombic antennas, ferrite rod, whip antennas. Receiving antennas, frequency independent antennas.

Wave Propagation:
Modes of Propagation: Surface Wave Propagation, Sky Wave (Ionospheric) Propagation- Virtual height, Maximum usable Frequency, Skip Distance, Optimum working frequency; Space Wave (Tropospheric) Propagation- line of sight distance.

Recommended Books

1. Antennas and Wave Propagation by G S N Raju, Pearson publications
2. Antennas and Radio Wave Propagation by K D Prasad Satya Prakashan
4. Antenna and Radio Wave Propagation by Krauss, TMH
5. Antenna and Radio Wave Propagation by Ballanis, john Wiley & Sons

SIXTH SEMESTER

Paper title: Advanced Microprocessors (Theory)

Paper Code: EC601 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A
8086 ARCHITECTURE: [4]
CPU Architecture, Internal operation, addressing modes, instructions formats, Instruction execution timing.

ASSEMBLY LANGUAGE PROGRAMMING: [7]
Assembler Instruction formats, Data Transfer, Arithmetic, Branch, loop, machine control, logical, Shift and rotate instructions, Directives and operators.

MODULAR PROGRAMMING: [4]
Linking & relocation, stacks, procedures, Interrupt and routines.

BYTE AND STRING MANIPULATION: [4]
String instruction, prefix, text editor, number format conversion.

I/O PROGRAMMING: [3]
Fundamental I/O consideration programmed I/O, Interrupt I/O, Block Transfer and DMA.

PART B

SYSTEM BUS STRUCTURE: [5]
Minimum mode, Maximum mode system bus timing and bus standard.

NUMERIC DATA PROCESSOR: [8]
8087, NOP data types, Processor architecture

INTEL 386 AND 486 MICROPROCESSORS: [10]
Intel 386 Microprocessor, Intel 486 Microprocessor, 486DX Architecture, Register Organisation of 486 Microprocessor, memory organization, Virtual Memory, Memory Management Unit(MMU), Interrupts and Exceptions, Addressing Modes of 80486.

Recommended Books
Microcomputer Systems 8086/8088, Family Yu Cheng Liu and G.A.Gibson, PHI

REFERENCES
Intel's Microcontroller Handbook

Paper Title: Advanced Microprocessors (Practical)

Paper Code: EC651 Max. Marks: 50

List of Experiments
1. Write a program to load register A, B, C and D with same constant (e.g., A1). Try to optimize your program in such a way that you use the smallest number of program bytes. Test your program in single step mode.

2. Assume that 4 bytes of data restored at consecutive locations of the data memory starting at location X. Write a program that loads register E with(X) i.e. with data contained at memory location X, D with (X+1), C with (X+2) and B with (X+3+0)
(a) Use direct addressing mode (LDA)
(b) User register indirect addressing mode (M)

Test your program in single step mode.

3. (a) Write a program which tests the zero condition of data byte specified at data memory location X. If it is zero, a 00 should be stored at location X+1, otherwise FF.
(b) Write a program which tests the all–one–condition of data byte specified at date memory location X. If all the bytes are 1, store 01 at location X+1, otherwise 00.

4. Four bytes of data are specified at consecutive data memory locations starting X. Write a program which increments the value of 4 bytes by 1.

5. Two unsigned binary numbers are stored at consecutive data memory locations, X+1. Write a program for computing (X+1)-(X). The magnitude of the result should be stored at Y and the sign 00 if positive and 01 if negative at Y+1.

6. (a) A double precision number, i.e. a 16 bit unsigned number, is stored X and X+1, with low order byte at X. Another double precision number is stored at Y and Y+1. Add the two numbers and store the result a W and W+1.
(b) Same as (a). Subtract the two numbers and store the result at W and W+1.

7. A code word is stored at memory location X. Write a program for testing whether the code word belongs to 2/5 code, and set the location Y to FF if yes 00 if no. The code word is valid if three MSBs are zero and if the number if 1’s in the remaining 5 bits is 2 (2/5 Code).

8. A counter is defined as register (e.g. B) which gets decremented till zero. Define such a counter as subroutine. Write a program, which consist of two counters, You must implement the following steps
   1. Set initial value of counter to 1.
   2. Call counter subroutine.
   3. Set initial value of counter to 2.
   4. Call counter subroutine.
   5. Go back to step 1.

9. (a) N binary numbers are stored at consecutive data memory locations, starting at X, where N is defined at data member location “NUMBER”. Find the largest number and display it in the data field.
(b) N binary numbers are started consecutive data member locations starting at X. Rearrange the numbers in ascending order.

10. A binary number is stored at data member locations X. Multiply the number by 10 and display the result in the address field (Hint: bx10=bx2 +bx8, a multiplication by 2 corresponds to a shift left on a bit).

11. An 8 bit binary number is stored at data memory locations. Y. Convert the decimal (BCD) and display the result in the address field.

12. Given 2 digit decimal number at data memory location X and X+1. Find the product using binary multiplications and display the result in address field.

13. Write a program for moving a data block starting a address X to address Y. The address X, Y as well as the block length are specified at some suitable data memory locations.

14. Write a program for moving a data block starting a address X to address Y. The address X,Y as well as the block length are specified at some suitable data memory locations.
15. A two digit BCD number is stored at memory location X. Convert the number into binary and display the result in data field.

16. Divide a 16 bit number by a 8 bit number and display the result in data field.

17. Write a program for display of decimal numbers 00-99 in sequence with a delay of 15 seconds between any two consecutive numbers.

Paper Title: Microwave Engineering (Theory)

Paper Code: EC602 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Waveguide Components [10]
Transitions, Discontinuities, Matched loads, Shorts, Flanges, Bends & Twists.
Attenuator & phase shifters, Microwave Hybrid Circuits: Waveguide Tees, Magic (Hybrid) Tees, Scattering matrix of tees, Hybrid Rings (Rat-Race Circuits), Directional Couplers: Two Hole Directional Couplers, Scattering matrix of a directional coupler, Hybrid Couplers, Multi-hole couplers.
Propagation in ferrites, Faraday rotation, Microwave Circulators: 3+0 port circulators and Isolators, YIG filter rectangular, Microwave cavities: Rectangular, Cylindrical Cavity Resonators, Q-factor of cavity resonator, aperture coupled cavity.

Measurements [5]
Slotted waveguide, Vector Voltmeter, Swept Frequency Technique Detectors, Power & Impedance measurement.

Solid State Sources – I [8]
Microwave BJTs, Heterojunction Bipolar Transistors (HBTs) and Tunnel Diodes.
Metal-Semiconductor Field Effect Transistors (MESFET), High Electron Mobility Transistors (HEMT). Transferred Electron Devices (TEDs) : GUNN Diode , LSA Diodes.

PART B


Microwave Tubes [12]
Microwave Linear Beam Tubes: Klystron, Multicavity Klystron, Reflex Klystron, Helix Traveling-Wave Tubes (TWT), Coupled Cavity Travelling-Wave Tubes. Microwave Crossed-Field Tubes: Cylindrical Magnetron.

Microwave Transmission Lines [6]
Strip Lines: Introduction, Microstrip Lines, Parallel Strip Lines, Coplanar Strip Lines and Shielded Strip Lines

Recommended Books


Paper Title: Microwave Engineering(Practical)

Paper Code: EC652

Max. Marks: 50

List of Experiments

4. Measurement of SWR.
5. Reflex klystron mode curves.
6. Antenna radiation pattern.
7. Verify Diode law.
8. Gunn Oscillator characteristics.
9. Directivity & Coupling of a directional coupler
10. To verify the waveguide law.

Paper title: Computer Networks (Theory)

Paper Code: EC603

Max. Marks: 100

Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

INTRODUCTION

[5]

PHYSICAL LAYER

[5]
Data Communication concepts, Wired and Wireless transmission media, Transmission Impairments and Performance, Introduction to PSTN, Switching, Circuit Switching and Packet Switching, Virtual Circuits.
DATA LINK LAYER
Data link layer Design Issues, Framing, Error Detection and Correction, Flow Control, Sliding Window Protocols, HDLC, SLIP, and PPP.

MEDIUM ACCESS CONTROL SUBLAYER
Channel Allocation, ALOHA, Slotted ALOHA, CSMA, CSMA/CD, IEEE LAN Standards: Ethernet (802.3), Gigabit Ethernet, Wireless LAN (802.11), Broadband Wireless (802.16), Bluetooth.

PART B
NETWORK LAYER
Network layer Design Issues, Routing algorithms—Shortest path, Flooding, Distance Vector Routing and Link State Routing; General principles of Congestion Control, Congestion Control in Datagram and Virtual Circuit Subnets, Brief idea of Quality of Service, Internetworking, IP protocol, IP Addresses, Internet Control Protocols, Subnetting and Super netting, NAT, DHCP, IPv4 and IPv6.

TRANSPORT LAYER
The Transport Service, Elements of Transport Protocols, TCP & UDP Protocols

APPLICATION LAYER
Brief Introduction to DNS, SMTP, FTP, TELNET, HTTP, WWW, SNMP and Cryptography.

Recommended Books

Paper Title: Computer Network (Practical)

Paper Code: EC653 Max. Marks: 50

List of Experiments:

1. To familiarize with the basic tools (crimping) used in establishing a LAN.
2. To study various topologies for establishing computer networks.
3. To familiarize with switch (manageable & Unmanageable) Hub, connectors, cables used in computes Networks.
4. To familiarize with routers & bridges.
5. To use basic commands like ping, trace-root, ipconfig, arp for troubleshooting network related problems.
6. To use various utilities for logging in to remote computer and to transfer files from/to remote computer.
7. To develop a program to implement the hamming code.
8. To develop a program to compute check sum for an ‘m’ bit frame using a generator polynomial.
9. To develop a program for implementing sliding window protocols.
10. To develop a program to implement a routing algorithm.

11. Study the various commands used to configure a router.

12. Study the performance of ALOHA, Slotted ALOHA, Ethernet, CSMA/CD on Network simulator.

13. Study the performance of Hub, switch, Bridge and router on network simulator.

14. Study the performance of various routing algorithms on network simulator.

15. Study the effect of various traffic patterns on network simulator.

16. Study the effect of IP multicasting on network simulator.

Paper Title: Software Engineering and Project Management (Theory)

Paper Code: EC604 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Software Evolution

Project Management Concepts

Software Project Planning

Risk Management

Software Quality Assurance
S/w quality concept, SQA- Software quality assurance activities, reviews, SQA plan, ISO 9000, Quality standards, ISO approach to quality assurance systems. [6]

PART B

S/W Configuration Management
Baselines, S/w configuration Items, SCM process, Version control, Change control. [5]

Design
Design Concepts and principles, Modular Design, Design Methods [6]

S/W Testing Methods
Testing Fundamentals, test case design, White box testing, Black Box testing, Testing Strategies, Verification & validation, Unit, Integration, Validation, System Testing. (6)

**Computer aided S/W Engineering**
CASE, Building blocks For CASE, Integrated CASE Environment. [4]

**Recommended Books**

**Reference Books**
Software Engineering by Ian Somerville (Addison Wesley), Edi 7th.
Software Engineering by Jalote, Pearson, Edi 1st.

**Paper Title:** Control Systems
**Paper Code:** EC605  Max. Marks: 100  Time: 3 hours

**Course duration:** 45 lectures of one hour duration each
**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**

**INTRODUCTION:**
History of automatic control, servomechanism, regulating systems, open loop, closed loop control systems, feedback, effect of feedback, linear and non linear control systems, block diagrams, Examples: speed control system, robot control system, temperature controls system, traffic control system, business control systems etc.

**MODELING:**
differential equations of physical systems, electrical, mechanical, translational, rational, gear systems, thermal systems. Electrical, mechanical analogies. Laplace transforms, transfer function. Block diagram algebra, signal flow graphs. characteristic equation Control system components: error detectors potentiometer, synchros, stepper motor, ac and dc techogenenrators.

**TIME DOMAIN ANALYSIS:**
Typical test input signals, Transient response of the first order, second order system, Time domain specifications Dominant closed loop poles of higher order systems, Steady state error and error coefficients.

**STABILITY:**
Concepts of absolute and relative stability pole zero location, routh Hurwitz criteria.

**ROOT LOCUS TECHNIQUE:**
Introduction, Root Locus Concept, Construction Root Loci, Stability analysis.

**PART B**

**FREQUENCY RESPONSE:**
Introduction, bode diagram, polar plots, log magnitude vs. phase plot, nyquist stability criterion, stability analysis, relative stability, Gain margin & Phase margin close loop frequency response.

**INTRODUCTION TO DESIGN:**
Necessity of compensation, lag and lead compensation, design of PID Controller.

**STATE SPACE ANALYSIS:**
Concept of State, state variable and state vector, state space modeling of continuous time and discrete time systems, solution of state equation, concepts of controllability and observability, pole-placement design.

**Recommended Books**

**References**
2. K. Ogata, Modern Control Engineering, PHI

**Paper Title: Operations Research**

**Paper Code: EC-606**

Maximum Marks: 100  
Time of examination: 3hrs.

Course Duration: 45 lectures of one hour each.

Note for the paper setter: Total of 8 questions may be set covering the whole syllabus. Candidate will be required to attempt any 5 questions selecting at least two from each part.

Syllabus:

PART A

**Optimization Problems.** Linear Programming: Graphical Method (Scope as in Chapter 1 of Reference 1).
Solution of simultaneous linear equations: An overview (Scope as in Chapter 2, Sections 2.15 – 2.16 of Reference 1).
Basic solutions, lines and hyperplanes, convex sets, extreme points, convex sets and hyperplanes (Scope as in Chapter 2, Sections 2.19 – 2.21 of Reference 1).
Reduction of any feasible solution to a system of equations to a basic feasible solution. Simplex Method: The simplex algorithm (Scope as in Chapter 3, 4 of Reference 1).
Tableau format for simplex computations, Charne’s M-method, Two phase method (Scope as in Chapter 5 of Reference 1).
The revised simplex method (Scope as in Chapter 7 of Reference 1).

(12 Lectures)
Duality theory: Formulation of the dual problem, Theorems on duality: Weak Duality Theorem, Strong Duality Theorem, Complementary Slackness Theorem, Dual Simplex Algorithm (Scope as in Chapter 8, Sections 8.1 – 8.12 of Reference 1). (6 Lectures)

Integer Linear Programming: Branch and Bound Algorithm, Cutting Plane Algorithm (Scope as in Chapter 9, Section 9.1 – 9.2 of Reference 2). (4 Lectures)

**PART B**

Transportation Problem: Initial solution by North-West corner rule, Row minima method, Column minima method, Matrix minima method, Vogel’s method. Tableau of transportation problem, u-v algorithm for solving transportation problem. Degeneracy in transportation problem. (Scope as in Chapter 9 of Reference 1). (6 Lectures)

The Assignment Problem: Hungarian Method (Scope as in Chapter 5, Section 5.4 of Reference 2). (2 Lectures)

**Traveling Salesman Problem** (Scope as in Chapter 9, Section 9.3 of Reference 2). (2 Lectures)

**Dynamic Programming**: Shortest route problem, Knapsack Model, Workforce size model, Equipment replacement model, Investment model, Game of chance (Scope as in Chapter 10, Sections 10.1 – 10.3, Chapter 15, Section 15.1 – 15.2 of Reference 2). (6 Lectures)

**CPM and PERT**: Network representation, Critical path computations, Construction of time schedule, Linear programming formulation of CPM, PERT networks (Scope as in Chapter 6, Section 6.6 of Reference 2). (2 Lectures)

**Basic Queuing Systems**: Elements of a queuing model, Pure birth and pure death model, Generalized Poisson queuing model (Scope as in Chapter 17, Section 17.1 to 17.5 of Reference 2). (5 Lectures)

References:


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**SEVENTH SEMESTER**

**Paper Title**: VLSI DESIGN (Theory)

**Paper Code**: EC 701  
Max. Marks: 100  
Time: 3 hours

**Course duration**: 45 lectures of one hour duration each

**Note for paper setter**: Total of Eight questions may be set covering the whole syllabus taking *four* from Part A & *four* from Part B. Candidates will be required to attempt any *five* questions taking at least two from each Part.

**Part A**
1. **Introduction to MOS Technology** (5)
   Basic MOS transistors, Enhancement and Depletion mode transistors, nMOS fabrication.

2. **MOS Circuits** (7)
   Parameters, Pass Transistor, nMOS inverter, CMOS inverter, MOS transistor circuit model, Latch up in CMOS circuits, Basic gates, depletion and enhance mode pull ups.

3. **MOS circuit Design Processes** (10)
   MOS layers, Stick Diagrams, nMOS design style, CMOS design style, Design rules and layout, Lambda based design rules, contact cuts, Double Metal MOS process rules, CMOS lambda-based design rules.

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**Part B**

4. **Circuit Characterization** (8)
   Resistance estimation, Capacitance Estimation, Power dissipation, Inverter delays, super buffers, propagation delays, Charge sharing.

5. **CMOS Design Methods and Testing** (10)
   Design strategies, CMOS chip design options, the need for testing, Design strategies for test, Chip-level test techniques.

6. **VLSI TOOLS** (5)
   Role of CAD tools in VLSI design process, Hierarchy of simulation tools, tanner tool, CMOS Layout tool: Microwind.

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**Recommended Books**


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**Paper Title:- VLSI DESIGN (Practical)**

**Paper code: EC 751**

Max. Marks: 50

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**List of Experiments (T-SPICE)**

1. Introduction to Tanner tool.
3. Transient analysis of NOR, OR.
4. Transient analysis of NAND, AND.
5. DC and AC analysis of Inverter.
6. DC and AC analysis of Common source amplifier configuration.
7. DC and AC analysis of basic MOS based current mirror.

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**References**

Paper Title: Digital Signal Processing

Paper code: EC 702  
Max. Marks: 100  
Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any fire questions taking at least two from each Part.

PART A

Continuous Time Signals [04]
Review of Fourier series and Fourier Transform, Sampling of Continuous Time signals.

Discrete Time Signals [08]
Discrete time Signals & Systems, Linear Time Invariant systems, Stability and Causality, Solution of Linear constant coefficient difference equations, Convolution, Correlation, Z-Transform and its properties, Inverse Z transform.

Frequency Domain Representation of Signals & Systems [10]

PART B

Digital Filters [10]
Ideal Filter vs. Practical Filters, General Specifications and Design Steps, Comparison of FIR & IIR Filters.

Design of FIR Filters: Window technique, Frequency sampling technique.

Design of IIR Filters: Impulse Invariance technique, Bilinear Transformation, Design of IIR Filters using Butterworth, Chebyshev and Elliptic filter, Digital frequency transformation.

Implementation of Discrete Time Systems [05]
Block diagrams and signal flow graphs for FIR and IIR systems. Direct form, Cascade and Frequency Sampling Structures for FIR systems, Direct forms, Cascade and Parallel form realization of IIR systems, Finite Word Length Effects.

DSP Processors [08]
Introduction to fixed point and floating point processors and their architecture, TMS320C5X Architecture, Memory, Addressing Modes, Interrupts and Assembly Language Programming.

Recommended Books

Paper Title: Digital Signal Processing (Practical)

Paper code: EC 752  
Max. Marks: 50

List of Experiments:
1. Introduction to MATLAB.
2. Generating & Plotting Discrete time signals.
3. Study the effect of noise on signals in MATLAB.
4. Inverse Z Transform.
5. Convolution of Causal & Non Causal sequences in MATLAB.
6. Auto & Cross-Correlation in MATLAB.
8. System Response to Arbitrary Inputs.
9. DFT & IDFT of two sequences.
10. FFT of two Sequences.
11. Circular Convolution.
12. FIR Filter Design using Window Method in MATLAB.
13. IIR Filter Design using Bilinear Transformation in MATLAB.
14. IIR Filter Design using Impulse Invariance in MATLAB.
15. Butterworth and Chebyshev Digital IIR Filters in MATLAB.
17. Study of DSP kits.

Paper Title: Optical Communication (Theory)

Paper code: EC 703  
Max. Marks: 100  
Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Overview of Optical Fibre Communication: -
Elements of basic communication system, communication system architecture, advantages of optical communication, Definition of dB and dBm.

Optical Fibre Wave Guides: -
Ray Theory of Transmission: Total Internal reflection, Acceptance Angle, Numerical Aperture, Electromagnetic mode theory for optical communication of both types of fibers viz step index fiber and graded index fibres.

Signal Degradation In Optical Fibres: -
Attenuation, Material absorption losses, linear and non linear scattering losses, fiber bend loss, dispersion viz intermodal dispersion and intramodal dispersion, overall fiber dispersion and polarization mode dispersion, Introduction to nonlinear effects: Self phase modulation, cross phase modulation, Stimulated Brillion and Raman scattering, Four Wave Mixing.

PART B

Optical Sources And Detectors: -

[03]  
[06]  
[10]
Sources: Basic principle of surface emitter LED and edge emitter LED- material used, structure, internal quantum efficiency and characteristics. LASER Diode - material used, structure, internal quantum efficiency and characteristics, working Principle and characteristics of Distributed feedback (DFB) laser.

Detectors: PIN photodiode - material used, working principle & characteristics, Avalanche Photodiode: - material used, working principle and characteristics.

Digital And Analog Transmission System: [12]
Overview of Analog Links, Carrier to Noise Ratio, Multichannel Amplitude & Frequency Modulation. Point to point Digital links, link power budget, Rise time budget, Introduction to Principle of WDM, Basic Application and types of Optical Amplifiers, Semiconductor Optical Amplifier, Erbium doped fiber amplifiers, Amplifier Noise.

Optical Fiber Measurements: - [04]
Test Equipments: Optical Power Meter, optical attenuator, Attenuation Measurements: Cutback technique, Insertion losses Method, Optical Time domain Reflectometer (OTDR), OTDR Trace, Eye Patterns.

Recommended Books
2. Optical Fiber Communication Principles & Practice by John M. Senior, PHI Publication

Reference Books
2. G.P Agrawal, “Fiber Optic Communication” Wiley Publisher

Paper Title: Optical Communication (Practical)

Paper code: EC 753 Max. Marks: 50

List of Experiments
1. To study the propagation loss and bending loss in optical fiber.
2. To set up a fiber optic analog link.
3. To set up a digital fiber optic link.
4. Study of intensity modulation technique using analog and digital input signal.
5. To study the frequency modulation and demonstrate voice transmission through optic fiber using FM.
6. Measurement of optical power and propagation loss using optical power meter.
7. To determine the bit rate supported by the fiber optic link.
8. To study the characteristics of PIN diode.
9. To demonstrate the concept of WDM system.

Paper title: Embedded System Design (Theory)

Paper Code: EC704 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Introduction Review of Embedded Hardware [10]

PIC Micro controller & Interfacing [15]

PART B [8]


Introduction to Real Time Operating Systems: Task And Task States, Tasks and Data, Semaphores and shared data [7]

Operating System Services: Message queues, Mailboxes and Pipes, Timer Function, Events, Memory Management, Interrupt Routines in an RTOS Environment, Basic Design Using RTOS.

Recommended Books

Paper Title: Advanced Digital Communication (Theory)

Paper code: EC 705 Max. Marks: 100 Time: 3 hours
**Course duration**: 45 lectures of one hour duration each

**Note for paper setter**: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**Rationale**: This course will familiarise the students with the design principles of modern digital communication systems using as models mobile telephony, coder and modulator designs. A detailed study of the principles of Multiple Access Techniques for Multi-user Communications will enhance their skills to define, design and evaluate digital communication systems.

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**PART A**

**Digital PAM**: binary PAM formats, line coding, bandlimited digital PAM systems, Nyquist pulse shaping, equalization, synchronization techniques, bit and frame synchronization. Coded pulse modulation, voice digitization rate (VDR) of PCM, DPCM, DM, ADM, CVSD, log PCM, their performance comparison, VDR reduction by speech coding, VOCODERS, noise performance of PCM and DM, Digital multiplexes. AT & T and CCITT hierarchies, quasi-synchronous multiplexes.

**Matched, correlation** and optimum filters and symbol error rate. [4]

**Access Technologies**: Digital Subscriber line, Fiber, Cable, Broadband fixed wireless access. [2]

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**PART B**

**Digital CW modulation**: BPSK, DPSK, QPSK, M’ary PSK, QASK, BFSK, Doubinary encoding, QPR coherent and non-coherent systems, error probabilities in PSK, DPSK, FSK, QPSK, 16 QAM, MSK, QPR and bit. [12]

**Spread Spectrum techniques**: DS, CDMA, FH, PN sequence, Power requirement, PN- sequence code, and Walsh’s code. [6]

**ISDN**: ISDN structure, Basic & Primary rate access, ISDN services. [3]

**Signalling**: In-Channel & common channel signalling, SS7. [2]

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**Recommended Books**


**Paper Title: RADAR ENGINEERING (Theory)**

**Paper code**: EC 706  
**Max. Marks**: 100  
**Time**: 3 hours

**Course duration**: 45 lectures of one hour duration each

**Note for paper setter**: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

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**PART A**
Radar Fundamentals


Radar Signal Processing: Moving Target Indicators & Doppler Processing


The Radar Equation


PART B

Targets & Interfering Signals

Radar cross-section (RCS), Definition & Fundamentals, RCS Fluctuations, Target Fluctuation Models.

Target Echo Information Extraction

Ranging, Target Velocity (Doppler Shift), Range & Velocity with CW & Pulse Doppler Waveforms, Radar height-finding.

Radar Antennas


Recommended Books

1. Radar: Principles, Technology, Applications by Byron Edde (Pearson Education)
2. Introduction to Radar Systems by Skolnik (Mc Graw Hill)
3. Microwave and Radar Engg by M. Kulkarni, Umesh Publications

Paper Title: Web Technologies (Theory)

Paper Code: EC 707 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Internet and World Wide Web:

Introduction, Internet Addressing, ISP, types of Internet Connections, Introduction to WWW, WEB Browsers, WEB Servers, URLs, http, WEB applications, Tools for WEB site creation.

HTML:

Introduction to HTML, Lists, adding graphics to HTML page, creating tables, linking documents, frames, DHTML and Style sheets
Java Script: [11]
Introduction, programming constructs: variables, operators and expressions, conditional checking, functions and dialog boxes, JavaScript DOM, creating forms, introduction to Cookies.

PART B

Java: [16]
Introduction to java objects and classes, control statements, arrays, inheritance, polymorphism, Exception handling, Multithreading, Building the Java Applets, Boxes, Radio Button, Managing Multiple controls, Scrollbars, Choice controls, Scrolling lists, Windows, Menu and Dialog Boxes, Pop up Windows, Graphics in Java, Mouse events, Drawing Objects, Fonts, Canvases, Images, Image maps, Graphics, Animation.

XML: [7]
Why XML, XML syntax rules, XML elements, XML attributes, XML DTD displaying XML with CSS.

Recommended Books

3. Web Enabled Commercial Application Development, by Ivan Bayross, BPB.

EIGHTH SEMESTER

Paper Title: Computer Architecture & Organization (Theory)

Paper code: EC 801 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

Objectives: This course offers a good understanding of the various functional units of a computer system and prepares the student to be in a position to design a basic computer system. Finally the student will be exposed to the recent trends in parallel and distributed computing and multithreaded application.

PART A

Register Transfer and Micro-Operations [6]
Register Transfer Language, Inter Register Transfer Arithmetic, Complements, fixed and floating point Representation, Micro-Operations, Shift Micro-Operations and Control Operations.

Basic Computer Origination and design [6]
Instruction Codes, Computer Instructions, Timing and Control, Execution of Instructions, Input, Output and interrupt, Design of Computer.
Computer Software

Control Processor Organization
Processor Bus Organization, ALU stack Organization, General Register Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Microprocessor Organization, Pipelining, Parallel Processing.

PART B

Micro program Control Organization
Control Memory, Address Sequencing, Micro program Sequences, Microinstruction Formats, and Software Aids.

Arithmetic Processor Design
Comparison and Subtraction of unsigned Binary Numbers, Addition, Subtraction, Multiplication, Division Algorithm, Processor configuration and control

Input-Output & Memory Organization
Input-Output interface, Asynchronous Data Transfer, DMA, Priority Interrupt, I/O Processor, Virtual Memory, Cache Memory, Associative memory, Memory Management Hardware.

Recommended Books
M. Morris Mano, Computer system & Architecture, Pearson Education

References
2. M. Morris and Charles R. Kinre, Logic and computer design Fundamentals, Pearson Education

Paper Title: Wireless Communication (Theory)

Paper code: EC 802 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

Rationale:
This course will familiarize the students with latest wireless communication techniques and the evolution in wireless communication systems from the 1G to 3G. A detailed study of Wireless system designing, modulation techniques, Wireless networking will broaden their thoughts in a wireless communication.

PART A

INTRODUCTION
Evolution of Mobile Communication Systems, Paging systems, cordless telephone systems, cellular telephone systems, comparison of common wireless communication systems, 2G cellular networks, 2.5 G
wireless network, HSCSD, GPRS, EDGE technology, 3G wireless network, UMTS, 3G CDMA2000, 3G TD-SCDMA, Wireless Local Loop, Blue tooth and Personal Area Networks.

SYSTEM DESIGN FUNDAMENTALS [9]
Frequency reuse, Channel alignment strategies, handoff strategies, interference and system capacity, improving coverage and capacity in cellular systems, parameters for mobile multipath channel, Small scale fading.

MODULATION TECHNIQUES [10]
Amplitude modulation, Angle Modulation, Digital Modulation, Linear modulation techniques, Constant envelope modulation, spread spectrum modulation techniques, Equalization, Equalizers in communication receiver, Diversity techniques, RAKE receiver, Fundamentals of channel coding

MULTIPLE ACCESS TECHNIQUES [3]
FDMA, TDMA, CDMA, SDMA

WIRELESS NETWORKING [4]
Difference between wireless and fixed telephone networks, development of wireless networks, ISDN

WIRELESS SYSTEMS [7]
GSM, GSM architecture, CDMA digital cellular standard, IS-95 system.

Recommended Books
Wireless Communications Principles and practice by Theodore S. Rappaport, Prentice Hall India

References

1. Modern Wireless Communications by Simon Haykin , Michael Moher , PHI
2. Wireless Communication and Networking By Jon W Mark, PHI

Paper Title: Wireless Communication (Practical)

Paper code: EC 852 Max. Marks: 50

Note: Students are required to perform experiments from any six blocks by selecting atleast two from each sub-block.

List of practicals

1. Equipment orientation
   (i) Familiarisation with spectrum analyser , simulation softwares, various kits to be used in the laboratory.
   (ii) Review of working of function generator , CRO , multimeter & other instruments.

2. Simulation and implementation of baseband digital signals
   (i) Types of baseband signals: unipolar, polar, bipolar, RZ, NRZ, etc.
   (ii) Distortion and noise. Eye diagram.

3. Simulation and implementation of modulated digital signals
   (i) PSK, ASK and FSK modulations.
   (ii) Demodulation with envelope detection and synchronous.
   (iii) PSK differential modulation.
   (iv) Quadrature modulations (QASK and QPSK).
(v) QAM modulation.

4. Global System for Mobiles (GSM)
   (i) Cellular telephony. GSM Architecture.
   (iii) AT Commands
   (iv) working of GSM mobile station.

5. Multiple Access
   (i) Time division multiple Access
   (ii) Frequency division multiple access

6. Spread Spectrum communication systems
   (i) Pseudo-noise coders
   (ii) Direct sequence spread spectrum communication systems
   (iii) Frequency hopped spread spectrum communication systems
   (iv) CDMA wireless computer communication systems

7. Channel Characteristics
   (i) Multipath channel propagation characteristics
   (ii) Bit-error rate measurement

8. Wireless Networks
   (i) Bluetooth wireless network.
   (ii) Wi-Fi
   (iii) Wi-Max

Paper Title: Digital System Design (Theory)

Paper Code: EC803 Max. Marks: 100 Time: 3 hours

Course Duration: 45 lectures of one hour each.

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

Rationale:

With the incorporation of this subject, students are able to design, test and realize the minimized combinational and sequential circuits. In today’s world, where the miniaturization plays an important role, students by studying this subject would be able to realize a given circuit with minimum hardware and space requirement.

PART A

COMBINATIONAL CIRCUITS [20]

Error Correction and Detection: Error detection and correction techniques, Single error detection, Single error correction with double error
Fault detection and Location in combinational circuits: Different methods of detecting and locating Faults in combinational circuits.
PART B

SEQUENTIAL CIRCUITS

Synchronous circuits: Concept of state diagram and state table, state assignment, Analysis and synthesis of sequential circuits, designs of Next state decoder and output decoder, state reduction, Machine minimization of completely and incompletely specified machines.


Fault detection and Location in sequential circuits.

Recommended Books

1. Switching and Finite Automata Theory by Kohavi, TMH.
2. Switching Theory & Logic Design by Rao, Pearson Ed.
3. Digital circuits and Logic Design By Lee, PHI.

References

1. Computer Logic Design, Morris Mano, PHI
2. Switching circuits for Engineers, Marcus, PHI
3. Introduction to Digital systems, James Palmier, David Perlman

Paper Title: Digital System Design (Practical)

Paper Code: EC 853 Max. Marks : 50

List of Experiments

1. To Design and test the minimized circuit of Full Adder.
2. To Design and test the minimized circuit of BCD to Binary Converter
3. Implement decade counter using minimum number of gates
4. To test the minimized circuit of Decimal to BCD Encoder
5. Design and test hexadecimal to binary Encoder
6. Implement and test BCD to 7-Segment decoder
7. Design a sequence detector to detect a given sequence
8. Design and test twisted type ring counter
9. Implement the minimized circuit of Modulo-6 counter
10. To design, implement and test a 16 :4 multiplexer using logic gates.
11. To design, implement and test a 4:16 demultiplexer using logic gates.
12. Design & test Johnson Counter.
Paper Title: Neural Networks and Fuzzy Logic (Theory)

Paper code: EC 804  Max. Marks: 100  Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Fundamentals of Neural Networks  [7]

Supervised Learning  [10]
Learning and memory, Representation of perceptron, Linear separability, Perceptron Learning, Training of single layer and multi-layer, back propagation training algorithm, Applications of backpropogation, Universal function approximation.

Attractors Neural Networks  [8]
Introduction, Associative memory, Hopfield networks, Content addressable memory, Bidirectional associative memories.

PART B

ART Networks  [7]
Vector quantization & simplified ART architecture, Architectures & algorithms of ART1 & ART2 networks, Applications.

Self-organizing Feature Map  [6]
Introduction, Competitive learning, Maxican Hat networks, SOFM algorithm, Applications.

Fuzzy Logic  [7]
Basic concepts of Fuzzy Logic, Fuzzy vs Crisp set, Fuzzy uncertainty & Linguistic variables, membership functions, operations on fuzzy sets, fuzzy rules for approximate reasoning, variable inference techniques, defuzzification techniques, Applications of fuzzy logic, Fuzzy system design.

Recommended Books
1. Neural Networks – A Classroom Approach by Satish Kumar, TMH.
2. Neural Networks, fuzzy Logic, and Genetic Algorithms by Rajasekaran & Vijayalakshmi Pai, PHI.
5. Fuzzy Logic with engineering applications by Ross, Mc-Graw Hill.

Paper Title: Artificial Intelligence (Theory)

Paper code: EC 805  Max. Marks: 100  Time: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.
PART A


Problem solving techniques: State space search, control strategies, heuristic search, problem characteristics, production system characteristics, Generate and test, Hill climbing, best first search, A* search, Constraint satisfaction problem, Mean-end analysis, Min-Max Search, Alpha-Beta Pruning, Additional refinements, Iterative Deepening.

Planning: The Planning problem, planning with state space search, partial order planning, planning graphs, planning with propositional logic, Analysis of planning approaches, Hierarchical planning, conditional planning, Continuous and Multi Agent planning

PART B

Knowledge representation: Mapping between facts and representations, Approaches to knowledge representation, Propositional logic, predicate logic, Resolution, Resolution in proportional logic and predicate logic, Clause form, unification algorithm, procedural vs declarative knowledge, Forward vs Backward reasoning, Matching, conflict resolution, Non-monotonic reasoning, Default reasoning, statistical reasoning, fuzzy logic Weak and Strong filler structures, semantic nets, frame, conceptual dependency, scripts.


Recommended Books

5. DAN, W. Patterson, Introduction to AI and Expert Systems, PHI, latest Edition

Paper Title: Digital Image Processing (Theory)

Paper code: EC 806 Max. Marks: 100 Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Introduction [4]
Fundamental Steps in Image Processing, Elements of Digital Image Processing, Image Acquisition, Storage, Processing, Communication, Display.

**Image Perception** [8]
Structure of the human eye, light, luminance, brightness, contrast, image model, sampling and quantization-uniform and non uniform, basic relationships between pixels, imaging geometry, camera model, stereo imaging.

**Image Enhancement** [10]
Spatial domain methods, Frequency domain methods, Enhancement by point processing, histogram processing, image subtraction, image averaging, spatial filtering, smoothing filters, sharpening filters, Enhancement in the frequency domain, Color image processing.

**PART B**

**Image Transforms** [11]

**Image Compression** [12]

**Recommended Books**

1. Digital Image Processing, by William K. Pratt, TMH

**Paper Title: Nano Technology (Theory)**

**Paper code:** EC 807  
**Max. Marks:** 100  
**Time:** 3 hours

**Course duration:** 45 lectures of one hour duration each

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**

**Introduction to Physics of the Solid State:** [10]
Structure, Size dependence of properties, Crystal structures, Face-Centered cubic nanoparticles, Tetrahedrally Bonded semiconductor structures, Lattice Vibrations, Energy Bands, Insulators,
Semiconductors and conductors, Reciprocal Space, Energy Bands and Gaps of Semiconductors, Effective masses, Fermi surfaces, Localized particles, Donors, Acceptors and Deep Traps, Mobility, Excitons.

Properties of Individual Nanoparticles: [10]
Introduction to Semiconducting Nanoparticles, Introduction to Quantum Dots, wells, wires, Preparation of Quantum Nanostructures, Introduction to Carbon Nanotubes, Fabrication, Structure, Electrical properties, Vibrational properties, Mechanical properties.

Biological Materials: [6]
Biological Building Blocks, Nucleic Acids, Biological Nanostructures.

PART B

Tools: [10]
TEM, Infrared and Raman Spectroscopy, Photoemission and X-RAY spectroscopy, Electron microscopy, SPMs, AFMs, Electrostatic force Microscope, Magnetic force microscope

Nanoscale Devices: [9]
Introduction, Nanoscale MOSFET-planer and non planer, Resonant-tunneling diodes, Single electron transistor, Quantum-Dot, Nano-electrochemical systems, Molecular/Bimolecular electron devices,

Reference Books: 1. Nanotechnology: G.Timp, Bell Labs, Murray Hill, NJ(Ed.)
2. Introduction to Nanotechnology-Charless P. Poole, Wiley International