PANJAB UNIVERSITY, CHANDIGARH- 160014 (INDIA)

FACULTY OF ENGINEERING & TECHNOLOGY

SYLLABI

FOR

Bachelor of Engineering (Electronics & Electrical Communication)
Third-Eight Semesters
Examinations,2010-2011
# SCHEME OF EXAMINATION FOR BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)

## THIRD SEMESTER

<table>
<thead>
<tr>
<th>Theory Paper Code</th>
<th>Paper Title</th>
<th>Hours/Week</th>
<th>Marks</th>
<th>Int. Ass.</th>
<th>Hours/Week</th>
<th>Marks</th>
<th>Int. Ass.</th>
<th>Practical Paper Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC-301</td>
<td>Semiconductor Electronics</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>50</td>
<td>EC-351</td>
</tr>
<tr>
<td>EC-302</td>
<td>Electromagnetic Theory</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>EC-303</td>
<td>Filters &amp; Transmission Lines</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>50</td>
<td>EC-353</td>
</tr>
<tr>
<td>EC-304</td>
<td>Digital Electronics</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>50</td>
<td>EC-354</td>
</tr>
<tr>
<td>AS-301</td>
<td>Engineering Maths-III</td>
<td>3+1</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>EC-305</td>
<td>Object Oriented Programming</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>50</td>
<td>EC-355</td>
</tr>
<tr>
<td></td>
<td>Workshop</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WS-157</td>
</tr>
<tr>
<td></td>
<td><strong>Grand Total:</strong> 1250</td>
<td><strong>19</strong></td>
<td><strong>600</strong></td>
<td><strong>300</strong></td>
<td><strong>12</strong></td>
<td><strong>100</strong></td>
<td><strong>250</strong></td>
<td></td>
</tr>
</tbody>
</table>

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The table above outlines the scheme of examination for the Bachelor of Engineering (Electronics and Electrical Communication) for the third semester. It includes details such as the theory papers, practical papers, their respective codes, credit hours, and marks分配.
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EC401</td>
<td>Communication Theory</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>---</td>
<td>----</td>
<td>----</td>
<td>--------</td>
</tr>
<tr>
<td>EC402</td>
<td>Analog Electronics Circuits</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>50</td>
<td>50</td>
<td>EC-452</td>
</tr>
<tr>
<td>EC403</td>
<td>Microprocessors</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>50</td>
<td>50</td>
<td>EC-453</td>
</tr>
<tr>
<td>EC404</td>
<td>Communication Engineering</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>50</td>
<td>50</td>
<td>EC-454</td>
</tr>
<tr>
<td>EC405</td>
<td>Operating Systems</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>EC406</td>
<td>Data Structures &amp; Algorithms</td>
<td>3+0</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>25</td>
<td>EC-456</td>
</tr>
<tr>
<td>Grand Total: 1250</td>
<td></td>
<td></td>
<td>18</td>
<td>600</td>
<td>300</td>
<td>12</td>
<td>175</td>
<td>175</td>
</tr>
</tbody>
</table>
### SCHEME OF EXAMINATION FOR BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)

#### FIFTH SEMESTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EECE-501</td>
<td>Linear Control System</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>EECE-552</td>
</tr>
<tr>
<td>EECE-502</td>
<td>Micro Electronics</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>25</td>
<td>EECE-554</td>
</tr>
<tr>
<td>EECE-503</td>
<td>Antenna &amp; Wave Propagation</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>EECE-555</td>
</tr>
<tr>
<td>EECE-504</td>
<td>Advanced Microprocessor</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>25</td>
<td>EECE-556</td>
</tr>
<tr>
<td>EECE-505</td>
<td>Instrumentation</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>25</td>
<td>EECE-557</td>
</tr>
<tr>
<td>EECE-506</td>
<td>Numerical Analysis</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Software Lab</td>
<td>4</td>
<td>25</td>
<td>25</td>
<td>EECE-556</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vocational training</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>150</td>
<td>EECE-557</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Grand Total: 1250**

<table>
<thead>
<tr>
<th>Theory</th>
<th>Practical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours</td>
<td>18</td>
</tr>
<tr>
<td>Marks</td>
<td>600</td>
</tr>
<tr>
<td>Exam</td>
<td>300</td>
</tr>
<tr>
<td>Int. Ass.</td>
<td>13</td>
</tr>
<tr>
<td>Marks</td>
<td>100</td>
</tr>
<tr>
<td>Exam</td>
<td>250</td>
</tr>
<tr>
<td>Practical Paper Code</td>
<td>-</td>
</tr>
</tbody>
</table>
### SCHEME OF EXAMINATION FOR BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)

#### SIXTH SEMESTER

<table>
<thead>
<tr>
<th>Theory</th>
<th>Paper Title</th>
<th>Hours/Week</th>
<th>Marks Uni.</th>
<th>Int. Ass.</th>
<th>Hours/Week</th>
<th>Marks Uni.</th>
<th>Int. Ass.</th>
<th>Practical Paper Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>EECE-601</td>
<td><strong>System Design Electronics</strong></td>
<td>4</td>
<td>100</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>EECE-602</td>
<td>Microwave Engineering</td>
<td>4</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>40</td>
<td>60</td>
<td>EECE-652</td>
</tr>
<tr>
<td>EECE-603</td>
<td>Micro controller and Embedded Systems</td>
<td>4</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>40</td>
<td>60</td>
<td>EECE-653</td>
</tr>
<tr>
<td>EECE-604</td>
<td>VHDL Programming &amp; Technology</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>40</td>
<td>60</td>
<td>EECE-654</td>
</tr>
<tr>
<td>EECE-605</td>
<td>Power Electronics</td>
<td>4</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>40</td>
<td>60</td>
<td>EECE-655</td>
</tr>
<tr>
<td>EECE-606</td>
<td>Human Resource Management</td>
<td>3</td>
<td>50</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Grand Total: 1250</td>
<td></td>
<td>22</td>
<td>550</td>
<td>300</td>
<td>12</td>
<td>160</td>
<td>240</td>
<td></td>
</tr>
</tbody>
</table>
### SEVENTH SEMESTER

<table>
<thead>
<tr>
<th>Theory Paper Code</th>
<th>Paper Title</th>
<th>Hours/Week</th>
<th>Marks</th>
<th>Int. Ass.</th>
<th>Hours/Week</th>
<th>Marks</th>
<th>Int. Ass.</th>
<th>Practical Paper Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>EECE-701</td>
<td>Digital communication</td>
<td>4</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>75</td>
<td>50</td>
<td>EECE-751</td>
</tr>
<tr>
<td>EECE-702</td>
<td>Digital Signal Processing</td>
<td>4</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>75</td>
<td>50</td>
<td>EECE-752</td>
</tr>
<tr>
<td>EECE-703</td>
<td>Wireless and Mobile Communication</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>EECE-704</td>
<td>Elective-1</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>EECE-753</td>
</tr>
<tr>
<td>Seminar-1</td>
<td></td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>4</td>
<td>--</td>
<td>100</td>
<td>EECE-754</td>
</tr>
<tr>
<td>Minor Project</td>
<td></td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>6</td>
<td>100</td>
<td>100</td>
<td>EECE-755</td>
</tr>
<tr>
<td>Vocational Training</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grand Total: 1250</td>
<td></td>
<td>14</td>
<td>400</td>
<td>200</td>
<td>16</td>
<td>250</td>
<td>400</td>
<td></td>
</tr>
</tbody>
</table>

Elective-1
0pt any one from the following:

1. Neural network and Fuzzy Logic
2. Artificial Intelligence
3. Web Technologies
4. Radar Engineering
### EIGHTH SEMESTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EECE-801</td>
<td>Optical Fiber Communication</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>50</td>
<td>EECE-851</td>
</tr>
<tr>
<td>EECE-802</td>
<td>Computer Network</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>3</td>
<td>25</td>
<td>50</td>
<td>EECE-852</td>
</tr>
<tr>
<td>EECE-803</td>
<td>Elective-II*</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>EECE-804</td>
<td>Computer Architecture</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>EECE-805</td>
<td>VLSI Design</td>
<td>3</td>
<td>100</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td>Major project</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>6</td>
<td>100</td>
<td>100</td>
<td>EECE-854</td>
</tr>
<tr>
<td></td>
<td>Seminar-2</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>4</td>
<td>--</td>
<td>100</td>
<td>EECE-855</td>
</tr>
<tr>
<td>EECE-800</td>
<td>General Fitness</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td>Grand Total: 1250</td>
<td>15</td>
<td>500</td>
<td>250</td>
<td>16</td>
<td>150</td>
<td>350</td>
<td></td>
</tr>
</tbody>
</table>

Elective-II*

1. Digital Image Processing
2. Satellite Communication
3. Nano-Technology
SYLLABUS FOR
BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)
THIRD SEMESTER

Paper Title:- Semiconductor Electronics (Theory)

Paper Code: EC 301  Max. Marks: 100  Time: 3 hours

Course duration: 45 lecturers of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Transistor characteristics : [10]
Junction transistor, transistor current components, current gain, transistor as an amplifier, common emitter, common base, common collector configurations, Input & output characteristics in CE, CB & CC configurations, photo transistor & its characteristics, unijunction transistor & its characteristics.

Transistor at low frequencies: [08]
Graphical analysis of CE configuration two port devices and hybrid model, h-parameters, comparison of amplifier configurations of circuits.

Transistor biasing and Thermal stabilization : [08]
Concept of biasing & biasing of BJT circuits, Operating point, bias stability, stabilization against variation in Ico, Vbe, and β, thermal run away, thermal stability.

PART B

Field Effect transistor : [09]
Junction field effect transistor, JFET characteristics, pinch off voltage and equivalent circuit, MOSFETS their modes of operation and characteristics, equivalent circuit, biasing of FETS.

Power amplifiers : [10]
Classification of amplifiers, Class A large signal amplifier, second and higher harmonic distortion, transformer coupled amplifiers, Efficiency of amplifiers, Push pull amplifiers (class A & class B).

BOOKS RECOMMENDED :

1. Integrated Electronics, Millman & Halkias (Mc-Graw Hill)
2. Microelectronics Circuits, AS Sedra & KC Smith (OXFORD)
3. Electronics Devices & Circuit Theory, RL Boylestead & L Nashelsky (PHI)
4. Electronic Circuit Analysis & Design, Donald A. Neamen (TMH)
Paper Title: - SEMICONDUCTORS ELECTRONICS (PRACTICAL)

Paper Code: EC-351               Max. Marks: 25

Note: At least eight experiments are to be done.

List of Experiments

1. To study the specification sheet & draw the characteristics of transistor in CB or CE configuration.
2. To study the specification sheet & draw the characteristics of FET in CD or CC configuration.
3. To draw the frequency response of a single stage BJT amplifier.
4. To measure the voltage and current gain of a BJT amplifier.
5. To measure the distortion in the output of a push pull amplifier.

To simulate the following using P-spice

1. Frequency Response of a single state FET amplifier.
2. Voltage and current gain of BJT amplifier.
3. Distortion of a push pull power amplifier.

Paper Title: - ELECTROMAGNETIC THEORY (THEORY)

Paper Code: EC 302               Max. Marks: 100               Time: 3 hours

Course duration: 45 lecturers of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Maxwell’s equation:
Maxwell’s equations in their integral and differential forms, Maxwell’s equations in free space and in harmonically varying fields. Physical Interpretation and Boundary Conditions [8]

Plane waves in Dielectric and Conducting Media:
Conductors and Dielectrics, Wave equations in conducting and dielectric media, its solution, Skin effect, relaxation time, impedance of the conducting medium. Reflection and transmission of the wave at a boundary. Poynting Vector: application to energy Radiation, Velocities of propagation: group velocity, phase velocity, wave polarization. [16]

PART B

Guided Waves:
Wave Guides:
Rectangular and Circular waveguides: T.M. & T.E. Modes, Wave impedance and characteristics impedances, Attenuation factor and Q of waveguides.

BOOKS RECOMMENDED:
3. Antennas and Wave Propagation by G S N Raju, Pearson publications, Edition 1ST

Paper Title: - FILTERS AND TRANSMISSION LINES (THEORY)

Paper Code: EC -303\nMax. Marks: 100\nTime: 3 hours

Course duration: 45 lectures of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Impedance Functions and Networks functions:
Concept of complex frequency, Transform Impedance and transform circuits, Network functions for the one port and twp port, Calculation of network functions, poles and Zeros for Network functions, Restrictions on Poles and Zeros Locations for Driving Point and Transfer functions, Time domain behavior from Pole and Zero plot, Stability of Active networks [09]

Filter Synthesis:
Classification of filters, Characteristics, impedance (input & characteristic) and propagation constant of pure reactive network, Ladder Network, T-section, pie section, Pass and stop bands, Constant –K low pass and high pass filters, m-derived T and pie section, Design of k and m-derived filters, Band pass filters, band elimination filters, Composite filters. [12]

PART B

Two port Parameters:
Relationship of Two port variables, Short Circuit Admittance and Open circuit Impedance parameters, Transmission and hybrid parameters. [06]

Sinusoidal Steady State Analysis:
Network Synthesis for two terminal network, Foster and Cauer forms. [03]
Transmission Lines:
Line parameters, Inductance and capacitance of a line of two parallel conductors, inductance of coaxial line, Line of Cascaded T-section, Transmission line-general solution, Physical significance of the equations.; the infinite line, wavelength, velocity of propagation, waveform distortion, distortionless line, telephone cable, Reflection on a line not terminated in $Z_0$, Reflection constant, Line calculation, Input and transfer impedance, open and short circuited lines, Reflection factor and reflection loss, parameters of open wire line and coaxial line at high frequencies, constants for the line of zero dissipation, Voltage and currents on dissipationless line, standing wave nodes, standing wave ratio. Input impedance of dissipationless line, power loss in unmatched lines, single stub matching and smithchart.

Books Recommended:

- Networks, Lines and Fields by John D. Ryder, PHI, Edition 2ND
- Network Analysis by M.E. Van Valkenburg (PHI), Edtion 3+0RD.
- Circuit Analysis by Allan D. Krauss (West Publishing Company), Edition Latest

Paper Title: - FILTERS AND TRANSMISSION LINES (PRACTICAL)

Paper Code: EC-353 Max. Marks: 25

Note: At least eight experiments are to be done

List of Experiments

1. To Design & implement a constant K low pass / high pass filter.
2. To Design & implement a band pass filter.
3. To Design & implement a m-derived low pass / high pass filter
4. To Design & implement a composite low pass/ high pass filter.
5. To Measure the characteristics and attenuation of a Transmission line.
6. To Measure the input impedance of a Transmission line.
7. To Measure phase displacement between the current and voltage at input of Transmission line.
8. To Study the Frequency characteristics and stationary waves of a Transmission line.
9. To Measure Signal Phase shift along the line.
10. Fault localization within the line.
PART A
Introduction
Concept of digitisation, Representation of Logic, Logic Variables, Boolean Algebra, Boolean Expressions and minimization of Boolean expression using K-Map(up to five variables), Review of Logic Gates, design & Implementation of Adder, Subtractor, Multiplexer, DeMultiplexer, Encoder, Decoder, ROM, Digital Comparators, Code Converters using gate, multiplexers / decoders

Flip-Flops
A 1- bit memory cell, clocked & unclocked flip flop, S-R Flip-Flop, JK Flip-Flop, Race around Condition, Master Slave Flip-Flop, D&T type Flip-Flop

Counters & Shift Registers
Ripple Counters, Design of Modulo-N ripple counter, Presetable Counters, Up-Down counter, design of synchronous counters with and without lockout conditions, design of shift registers with shift-left, shift-right & parallel load facilities, Universal shift Registers

PART B
Data Converters
Sample & Hold switch, D/A converters: weighted resistor type, R-2R Ladder type; A/D Converters: Counter-Ramp type, Dual Slope Type, Successive approximation type, flash type; Specifications of ADC & DAC

Digital Logic families
Characteristics of digital circuits: fan in, fan-out, power dissipation, propagation delay, noise margin; Transistor-transistor Logic(TTL), manufacturer Data Sheets & Specifications, Types of TTL Gates (Schottky, standard, low power, high speed). Emitter Coupled Logic(ECL), Manufacturers Data sheets & Specifications, Comparison of Characteristics of TTL and ECL, Tristate Logic & its applications.

Semiconductor Memories & Programmable Logic
ROM, PROM, EPROM, EEPROM; RAM: Static RAM, Typical Memory Cell, Memory Organisation, Dynamic RAM cell, Reading, & Writing Operation in RAM, PLA, PAL & FPGA

BOOKS RECOMMENDED:

1. Digital Electronics by Taub Schilling
2. Integrated Electronics by Millman & Halkias
3. Digital System Principles & Applications by R J Tocci (PHI)
4. Digital Logic Design By Morris Mano
Paper Title: - DIGITAL ELECTRONICS (PRACTICAL)

Paper Code: EC-354 Max. Marks : 25

Note: At least eight experiments are to be done.

List of Experiments

1. To Study the data sheets of TTL and ECL gates
2. Verify the truth tables of with various gates, RS, D, JK Flip Flops
3. To design and implement a Modulo-N Counter
4. To Design and implement a Universal shift register
5. To perform arithmetic & Logic operations on two 4-bit binary numbers using an ALU.
6. To Transfer the Data between Three Registers through Tristate Circuit
7. To Understand Decoder/Driver and their applications with display. To display a count from 00 to 99 with a delay of N seconds.
8. Design & fabrication of synchronous counter
9. Design & fabrication of Combinational circuits using Multiplexers
10. To convert 8 bit Digital data to Analog value using DAC
11. To convert Analog value into 8 bit Digital data using ADC

Paper Title: Engineering Mathematics – III

Paper Code: AS301 Maximum Marks: 100 Time: 3hours.

Course duration: 45 lecturers of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

Part - A

Sequences and Series: (08)

Linear Algebra: (07)
Concept of linear independence and dependence, Rank of a matrix: Row – Echelon form, System of linear equations: Condition for consistency of system of linear equations, Solution by Gauss elimination method. Inverse of a matrix: Gauss – Jordan elimination method (Scope as in Chapter 6, Sections 6.3 – 6.5, 6.7 of Reference 1). Eigen values, eigen vectors, Cayley – Hamilton theorem (statement only). Similarity of matrices, Basis of eigenvectors, diagonalization (Scope as in Chapter 7, Sections 7.1, 7.5 of Reference 1).

Part - B

Complex Functions: (08)
Definition of a Complex Function, Concept of continuity and differentiability of a complex function, Cauchy – Riemann equations, necessary and sufficient conditions for differentiability (Statement only). Study of complex functions: Exponential function, Trigonometric functions, Hyperbolic functions, real and imaginary part of trigonometric and hyperbolic functions, Logarithmic functions of a complex variable, complex exponents (Scope as in Chapter 12, Sections 12.3 – 12.4, 12.6 – 12.8 of Reference 1).
Laurent Series of function of complex variable, Singularities and Zeros, Residues at simple poles and Residue at a pole of any order, Residue Theorem (Statement only) and its simple applications (Scope as in Chapter 15, Sections 15.1 – 15.3 of Reference 1).

Conformal Mappings, Linear Fractional Transformations (Scope as in Chapter 12, Sections 12.5, 12.9 of Reference 1).

BOOKS RECOMMENDED:


Paper Title: OBJECT ORIENTED PROGRAMMING (THEORY)

Paper Code: EC 305  Max. Marks: 100  Time: 3 hours

Course duration: 45 lecturers of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Principles Of Objected Oriented Programming
Advantages of OOP, comparison of OOP with Procedural Paradigm  [3]

C++ Constructs
Tokens, Expressions and control structures, various data types, and data structures, Variable declarations, Dynamic Initializations, Operators and Scope of Operators, Typecasting, Unformatted and formatted console I/O Operations  [3]

Functions
Classes and Objects: Prototyping, Referencing the variables in functions, Inline, static and friend functions. Memory allocation for classes and objects. Arrays of objects, pointers to member functio  [5]

Constructors And Destructors
Characteristics and its various types, Dynamic Constructors, Applications, Order of Invocation, C++ garbage collection, dynamic memory allocation.  [5]
Polymorphism
Using function and Operator overloading, overloading using friend Functions, type conversions from basic data types to user defined and vice versa. [5]

PART B

Inheritance
Derived classes, types of inheritance, various types of classes, Invocation of Constructors and Destructors in Inheritance, aggregation, composition, classification hierarchies, metaclass/abstract classes. [6]

Pointers
constant pointers, Use of this Pointer, Pointer to derived and base classes, virtual functions, Bindings, Pure virtual Functions and polymorphism [5]

I/O Operations And Files
Classes for files, Operations on a file, file pointers [4]

Generic Programming With Templates
Definition of class template, Function Templates, Overloading Template Functions, Class templates and member functions templates with parameters, Standard C++ classes, persistent objects, streams and files, namespaces, exception handling, generic classes, standard template library: Library organization and containers, standard containers, algorithm and Function objects, iterators and allocators, strings, streams, manipulators, user defined manipulators and vectors [6]

Introduction
Object Oriented System, Analysis and Design [3]

BOOKS RECOMMENDED:

1. Object Oriented Programming with C++ By Bala Guruswamy, TMH, Edition 3rd
3. The C++ Programming Language By Bjarne Stroustrup, Edition 3rd
5. The Complete Reference to c++ By Schildt, TMH, Edition 4th
6. OOPs Using C++ By Sanjeev Sofat, Khanna Publishions, Edition Latest

Paper Title: - OBJECT ORIENTED PROGRAMMING (PRACTICAL)

Paper Code: EC 355 Max. Marks: 25

Note: At least eight experiments are to be done

List of Experiments
1. Implementation of Functions, Classes and Objects
2. Constructors and Destructors
3. Operator Overloading and Type Conversion
4. Inheritance and Virtual Functions
5. Files
7. More experiments related to theory course.
SYLLABUS FOR  
BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)  

FOURTH SEMESTER  

Paper Title: - COMMUNICATION THEORY  

Paper Code: EC 401 Max. Marks: 100 Time: 3 hours  

Course duration: 45 lecturers of one hour duration each.  

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.  

PART A  

Signal & its Representations  

Random Signal Theory  
Sample space, random variables-discrete & Continuous, examples of probability Density Functions-Moments, joint & conditional PDF density functions of sums, Transformation, concept of correlation, auto & Cross-correlation functions, white Noise. [8]  

Transmission of Signals through Networks  

PART B  

Noise & Interference  
Classification of Noise, Sources of noises, atmospheric shots, Thermal noise, noise in Semiconductors, Noise spectral density, Noise calculations, Noise Figures of devices & circuits, cascaded networks, Minimum noise, Figures of networks. Experimental determination of Noise Factor [07]  

Basic Information Theory  
Concept Information, Entropies of Discrete Systems, Rate of transmission- Redundancy, Efficiency & Channel capacity, Source encoding including Huffman’s Technique, continuous Channel- Entropy maximization, Transmission rate of Channels, capacity of Noisy channels. Discussion of Shannon’s coding theorem, Comparison of Analog & Digital Communication Systems with reference to the Ideal Channel Capacity Theorem. [14]  

BOOKS RECOMMENDED:  
2. Introduction to Modern Communication by P D Sharma, Edition Latest
Paper Title: ANALOG ELECTRONIC CIRCUITS (THEORY)

Paper Code: EC 402 Max. Marks: 100 Time: 3 hours

Course duration: 45 lecturers of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Response of transistor Amplifier
Review Biasing, classification of amplifier, distortion in amplifiers, frequency & phase response of an amplifier, RC coupled amplifier, its low and high frequency responses, transistor model at high frequencies for CE and Emitter follower configuration, high frequency response of two cascaded CE transistor stages [9]

Feedback and Stability
Introduction to feedback, Basic-Feedback Concepts, Ideal Feedback Topologies, Voltage(Series-Shunt) Amplifiers, Current(Series-Shunt) Amplifiers, Transconductance(Series-Series) Amplifiers, Transresistance(Shunt-Shunt) Amplifiers,

Operational Amplifier
Differential Amplifier, Block diagram representation of a typical Op-amp, Interpreting of a typical set of data sheets, ideal op-amp, equivalent circuit, of op-amp, ideal voltage transfer curve, open loop op-amp configuration, the practical op-amp, input offset voltage, input bias current, input offset current, total output offset voltage, thermal drift, noise, common mode configuration, CMRR, Frequency Response, Frequency response of internally compensated Op-Amps, Frequency response of Non-compensated OP-Amps, Open loop voltage gain as a function of frequency, Closed loop frequency response, Slew rate [10]

PART B

Op-amp Applications
DC and AC Amplifiers, summing, Voltage–to-current converter, current to voltage converter, the Integrator, the Differentiator, Comparator, Zero-crossing detector, Voltage to frequency and frequency to voltage converters, Clippers and Clampers, Sample and Hold Circuit, Instrumentation Amplifier.

Active Filter, Oscillators & Tuned Amplifiers

BOOKS RECOMMENDED:

1. Electronics Circuit Analysis and Design by Donald A. Neamen, Tata McGraw Hill

3. Integrated electronics by Millman & Halkias

**Paper Title:** ANALOG ELECTRONICS CIRCUITS (PRACTICAL)

**Paper Code:** EC 452  
**Max. Marks:** 50

Note: At least eight experiments are to be done.

**List of Experiments**

1. To study the Pspice Simulation software
2. Design fabrication & testing of Differentiator Circuits using Op-Amp & simulate using P-spice
3. Design fabrication & testing of Integrator Circuits using Op-Amp & simulate using P-spice
4. Design fabrication & testing of adder/Subtractor Circuits using Op-Amp & simulate using P-spice
5. Design fabrication & testing of Clippers and Clampers Circuits using Op-Amp & simulate using P-spice
6. Design fabrication & testing of Universal Active filter & simulate using P-spice
7. To study the frequency response of OP-Amp & simulate using P-spice
8. To design Butter worth Low pass filter & simulate using P-spice
9. To design Butter worth High pass filter & simulate using P-spice
10. To design Butter worth Band pass filter & simulate using P-spice
11. To design Monostable & Free running Multivibrator using 555

**Paper Title:** MICROPROCESSOR (THEORY)

**Paper Code:** EC 403  
**Max. Marks:** 100  
**Time:** 3 hours

**Course duration:** 45 lecturers of one hour duration each

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**

**Microprocessor Architecture and Microcomputer Systems:**
Microprocessor Architecture Memory, Input and Output Devices, The 8085 MPU, Example of an 8085-Based Microcomputer, Memory Interfacing, The SDK-85 Memory System.  

**Interfacing I/O Devices:**

**Programming the 8085:**

**Programming Techniques with Additional Instructions:**

**PART B**

**Counters and Time Delays:**
Counters and Time Delays, Hexadecimal Counter, Modulo Ten, Counter, Generating Pulse Waveforms, Debugging Counter and Time-Delay Programs. [4]

**Stack and Subroutines:** Stack, Subroutine, Conditional Call and Return Instructions. [3]

**Interrupts:** The 8085 Interrupt, 8085 Vectored interrupts. [3]

**Interfacing Data Converters:**

**General –Purpose Programmable Peripheral Devices:**
The 8255A Programmable Peripheral Interface, Illustration: Interfacing Keyboard and Seven-Segment Display, Illustration: Bi-directional Data Transfer between Two Microcomputers, The 8254 Programmable Interval Timer, The 8259 A Programmable Interrupt Controller, Direct Memory Access (DMA) and the 8257 DMA Controller, serial communication, Programmable communications interface 8251. [8]

**BOOKS RECOMMENDED:**

4. Douglas V. Hall , “Microprocessors and Interfacing programming and Hardware, Edition 2nd

**Paper Title:- MICROPORCESSOR (PRACTICAL)**

**Paper Code: EC 453**

Max. Marks: 50

Note: At least eight experiments are to be done.

**List of Experiments**

1. Familiarization of 8085 kits.
2. Verification of arithmetic and logic operations using above kits.(At least 5 programs)
3. Development of interfacing circuits of various control applications based on 8085.
4. Application of assembly language using 8085 instructions set to develop various programs.
5. Applications of data movement instructions to develop relevant programs.

More experiments related to theory coarse.
Paper Title: COMMUNICATION ENGINEERING (Theory)

Paper Code: EC 404  Max. Marks: 100  Time: 3 hours

Course duration: 45 lecturers of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Amplitude Modulation & Demodulation and Systems

[15]

Frequency Modulation
Principles and generation of FM and PM signals, Reactance Modulator method, Armstrong Method, noise consideration in FM and PM system,

[7]

PART B

Frequency Demodulation and FM Systems
Detection of FM and PM signals, Foster Discriminator, ratio and PLL detectors, FM Transmitter (Block Diagram), FM receiver (Block Diagram), Pre-emphasis and de-emphasis circuit.

[8]

Pulse Modulation & Demodulation
Principles, generation and detection of PAM, PWM, PPM & PCM signals, noise in pulse modulation system, band width consideration, companding, delta modulation, adaptive delta modulation systems. TDM & FDM

[15]

BOOKS RECOMMENDED:


Paper Title: COMMUNICATION ENGINEERING (PRACTICAL)

Paper Code: EC 454  Max. Marks: 50

Note: At least eight experiments are to be done.

List of experiments
1. To measure the modulation index of AM signals using the trapezoidal method
2. To study DSB/SC AM signal and its demodulation using product Detector Circuit.
3. To study the voltages and waveforms of various stages of super-heterodyne receiver
4. To measure the sensitivity and selectivity of a super heterodyne radio receiver
5. To study the voltages and waveforms of various stages of FM Receiver
6. To study the pulse code modulation and de-modulation circuit
7. To study the Time division multiplexing and demultiplexing circuit
8. To study delta modulation and demodulation circuits.
9. To study sigma delta modulation and demodulation circuits.

Paper title: OPERATING SYSTEMS

Paper Code: EC405 Max. Marks: 100 Time: 3 hours

Course duration: 45 lecturers of one hour duration each
Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Concept of an operating systems, batch system, Multi-programmed, Time sharing, Personal Computer System, Parallel system, Real time system, General system Architecture.

System components, operating system services, System calls, System Programs, System Structure, System design and implementation. Concept of process, process states, process state transition, process control block, operations of processes, concurrent processes, deadlocks, scheduling algorithms, scheduling criteria, Process Synchronization.

Memory Management: [6]
Logical and physical address space, storage allocation and management techniques, swapping, concepts of multi programming, paging, segmentation, virtual storage management strategies, Demand Paging, Page Replacement Algorithms, Thrashing.

PART B

Information Management: [6]
File concept, Access method, Directory structure, Protection File system structure, Allocation methods, Free space management, Directory implementation, Disk structure, Disk Scheduling, Disk management, Swap space management.

Distributed-System Structures: [6]
Network operating system, Distributed operating systems, Remote services, Robustness, Design Issues.

Distributed file systems and Distributed Coordination: [6]

Case Studies: [5]
Unix O.S. Architecture, Operating system services, user perspective, representation of files in Unix system processes and their structure, Input-output system, Memory management, Unix shell, history and evolution of Unix system.

BOOKS RECOMMENDED:


REFERENCE BOOKS


Paper Title:- DATA STRUCTURES AND ALGORITHMS (THEORY)

Paper Code: EC 406 Max. Marks: 100 Time: 3 hours

Course duration: 45 lecturers of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Introduction: Introduction to data structures; Introduction to Algorithms Complexity;[1]

Arrays, Stacks & Queues: Concepts; Basic operations & their algorithms; Transverse, Insert, Delete, Sorting of data in these data structures; Prefix, Infix, Postfix Notations;[8]

Lists: Concepts of Link List and their representation; Two way lists; Circular link list; Basic operations & their algorithms: Transverse, Insert, Delete, Searching and Sorting of data in List; Storage Allocation & Garbage Collection; Linked stack and queues; Generalized List; sparse matrix representation using generalized list structure;[10]

PART B

Trees:
Binary Trees and their representation using arrays and linked lists; Trees and their applications; Binary tree transversal; Inserting, deleting and searching in binary trees; Heap & Heap Sort; General Trees; Thread binary tree; Height balance Tree (AVL); B-Tree;[08]

Graphs and their applications:
Graphs; Linked Representation of Graphs; Graph Traversal and spanning forests; Depth first search; Breadth first search;[08]

Sorting & Searching:
BOOKS RECOMMENDED:

2. Theory and problems of Data Structures Seymour Lipschutz (McGraw Hill), Edition 1st

Paper Title: DATA STRUCTURES AND ALGORITHMS (PRACTICAL)

Paper Code: EC 456 Max. Marks: 25

Note: At least eight experiments are to be done.

List of experiments

1. Implementation of array operations: Traversal, Insertion & Deletion at and from a given location; Sparse Matrices: Multiplication, addition.
2. Stacks: Implementation of Push, Pop; Conversion of Infix expression to Postfix, Evaluation of Postfix expressions.
4. Implementation of linked lists: inserting, deleting, and inverting a linked list. Implementation of stacks & queues using linked lists; Polynomial addition, Polynomial multiplication.
6. Graphs: BFS & DFS.
7. Implementation of sorting and searching algorithms
8. Hash tables implementation: searching, inserting and deleting, searching & sorting techniques
SYLLABUS FOR
BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)
FIFTH SEMESTER

Paper Title: - LINEAR CONTROL SYSTEM

Paper Code: EECE- 501  Max. Marks: 100  Time: 3 hours

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part

PART - A

1. Introduction [04]
Concepts Plant, Systems Servomechanism, regulating systems, disturbances, Open loop control system, closed loop systems, linear and non-linear systems, time variant &Invariant, continuous and sampled data control systems, Block diagrams, some illustrative examples.

2. Modelling [08]
Formulation of equation of Linear electrical, mechanical, thermal Pneumatic and hydraulic system, electrical, Mechanical analogies. Uses of Laplace transform, Transfer function, concepts of state variable modelling. Block diagram representation signal flow graphs and associated algebra, characteristics equation.

3. Time Domain Analysis [04]
Typical test - input signal, Transient response of the first and second order systems. Time domain specifications, Dominant closed loop poles of higher order systems. Steady state error and coefficients.

4. Stability : [06]
Concept of absolute and relative stability, Pole-zero location and stability. Routh-Hurwitz Criterion

PART – B

5. Root Locus Technique: [05]
The extreme points of the root loci for positive gain. Asymptotes to the loci, breakaway points, intersection with imaginary axis, location of roots with given gain & sketch of the root locus plot

6 Frequency Domain Analysis: [10]

7. Compensation: [04]
Necessity of compensation series and parallel compensations, Compensating network, application of lag and lead compensation.

8. Control Components: [04]
Error detectors- potentiometers and synchronous, servo motor A.C. and D.C. techno generators, Magnetic amplifiers.
BOOKS RECOMMENDED

1. Modern Control Engg. by K. Ogata, Prentice Hall, New Delhi
3. Automatic Control System by B.C. Kuo, Prentice Hall, 3rd Ed.

Paper Title: - MICRO ELECTRONICS (THEORY)

Paper Code: EC- 502  
Max. Marks: 100  
Time: 3 hours

Course duration: 45 lectures of one hour duration each

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part

PART - A

Introduction: [04]
General classification of Integrated circuits, advantages of IC’s over Discrete Components, Computer Generations.

Thick Film and Thin Film Hybrid ICs: [09]
Features of Hybrid IC technology, Thick film technology, Thick film processing. Thick film substrates, Thin film design, guidelines and applications of thick film hybrids. Thin film technology, thin film processing, thin film design, guidelines, advantages and applications of thin film hybrids.

Monolithic IC Processes: [14]

PART - B

Monolithic Components: [14]

Basic Building Blocks for ICs: [04]
Bipolar Transistor current sources independent of supply voltage variations.
Books Recommended:


Paper Title: - MICRO ELECTRONICS LAB

Paper Code: EECE-552 Max. Marks: 25

Note: At least eight experiments are to be done.

LIST OF EXPERIMENTS:

1. To analyze the failures in IC chips.
2. To study reliability of integrated circuits.
3. To study the basic IC process.
4. To study Micro-Electro Mechanical systems (MEMS).
5. To study the assembly and packing of IC.
6. To study the various connectors.
7. To study the various steps in PCB Design.
8. Project on PCB Design.
Paper Title: - ANTENNAS AND WAVE PROPAGATION (THEORY)

Paper Code: EECE- 503

Max. Marks: 100  Time: 3 hours

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part

PART - A

Radiation
Radiation from short current filament, radiation resistance, directivity and gain, radiation from a current loop, half wave dipole, antenna impedance, Experiment Folded dipole, monopole, BALLINS, one dimensional broadside and endfire arrays, multiplication of patterns, effect of earth on patterns.
Feed networks for array, yagi lida array, log-percotic arrays. Dolph-Techbyshfeff arrays.

Practical Antennas-
Top loading and tuning, effective heights, delta machine, rhombic antenna, ferrite rod, whip antenna, Receiving antennas, Antenna temperature, frequency independent antennas.

PART - B

Ground wave Propagation
Friis Free space equation, Reflection from earth’s surface, Surface and Space wave propagation for vertical and horizontal dipole, Field strength of Space wave, Range of space wave propagation, Effective earth’s radius, Effect of earth imperfections and atmosphere on space wave propagation, Modified refractive index, Duct propagation, Tropospheric propagation.

Ionospheric Propagation
Structure of ionosphere, propagation of radio waves through ionosphere, Refractive index of ionosphere, Reflection and refraction of waves by ionosphere, Critical frequency, Maximum usable frequency, Optimum working frequency, Lowest usable high frequency, virtual height, Skip Distance, Effect of earth’s magnetic field.

BOOKS RECOMMENDED:

PART – A

8086 Architecture: [06]
CPU Architecture, internal operation, addressing modes, instructions formats, instruction execution timing.

System Bus Structure: [06]
Pin diagram, Minimum mode, Maximum mode system bus timing

Assembly Language Programming: [06]
Assembler Instruction formats, data transfer, Arithmetic, Branch, Loop, machine control, Shift rotate and instructions. Directives and operators, String instruction, prefix.

Modular Programming: [06]
Linking & relocation, stacks, procedures, interrupt and routines.

PART – B

I/O Interfaces: [11]
8251 A programmable communication interface, 8255 A programmable peripheral interface, 8253 programmable interval timer, Interfacing a microprocessor to keyboard, Interfacing to alphanumeric displays, Keyboards/Display controller, DMA controller 8257, Serial data transmission methods & standards.

Memory Interfacing [06]
Memory mapped I/O, Programmed I/O, Memory organization, memory Banks, Interfacing with RAM, ROM & EPROM

Introduction to 80286, 80386 [04]

BOOKS RECOMMENDED:

LIST OF EXPERIMENTS:

1. To study the microprocessor Intel 8086 kit.
2. Write a Program to find the sum of two 32-bit Numbers.
3. Write a Program to find the multiplication of two 32-bit Numbers.
4. Write a Program to move a block of Data.
5. Write a Program to Find the no. of Even, Odd, Positive and Negative no. in the given array.
6. Write a Program to move a block of Data in the overlapping area.
7. Write a Program to arrange the given array into descending order using BUBBLE SORT Method.
8. Write a Program to convert BCD to equivalent Seven Segment Display (HEX) code (using look up table).
9. Write a Program to find the parity of a Multi-byte No.
10. Write a Program to solve a Given Logical Expression  $A + B' (C \oplus D)$
11. Write a Program to find the sum of two 16-digit Packed BCD Numbers and Result should also be a valid Packed BCD Number.
12. Waveform generation using 825
characteristics, application of thermistor. Thermocouple; construction, measurement of thermocouple output, compensating circuits, its advantages and disadvantages. LVDT: advantages and disadvantages and uses. Capacitive transducer for measurement of liquid level and frequency response, its advantages and disadvantages and uses. Piezoelectric transducer. Ultrasonic, optical, velocity, torque, pressure, temperature, flow, humidity, moisture & chemical sensors.

BOOKS RECOMMENDED:

3. WD. Cooper, “Electronic Instrumentation and Measurement Techniques”, Prentice-Hall.

Paper Title: - INSTRUMENTATION LAB

Paper Code: EECE -555 Max. Marks: 25

Note: At least eight experiments are to be done

LIST OF EXPERIMENTS:

1. Determination of characteristics of temperature sensor like RTD, Negative temperature coefficient thermistor, type K thermocouple.
2. Determination of Characteristics of light sensor like photo-voltaic cell, photo transistor, photo conductive cell, PIN photodiode.
3. Determination of Characteristics of displacement and force sensor such as LVDT, linear variable capacitor, strain gauge.
4. Determination of characteristics of air flow transducer.
5. Determination of characteristics of air pressure transducer.
6. Determination of characteristics of humidity transducer.
7. Determination of characteristics of sound transducer such as dynamic microphone, moving coil loudspeaker, buzzer.
8. Determination of characteristics of display device like LED bar graph display, moving coil meter.
9. To study Data Acquisition System.
10. Determination of frequency and phase angle using CRO.
PART – A

Solution of Algebraic and Transcendental Equations:

Conditions for the convergence of the iteration method, rate of convergence of the interactive method, comparison of false position, Newton-Raphson and secant methods, conversion of a divergent functional iteration scheme into a convergent one. Acceleration of convergence, Aitken’s Delta square process, error bonds, Newton-Raphson method for non linear system of equations.

Numerical Methods in Linear Algebra:
Computation of determinant, pivot, partial and complete pivoting technique, triangularization algorithm, triangular decomposition of a matrix, properties of triangular matrices, least squares curve fitting, solution of homogenous linear systems, matrix inversion, Gaussian elimination, factorization, Jacobi’s and Gauss-Siedel method, Solution of tridiagonal systems, Eigenvalues and eigenvectors of a matrix, Cayley Hamilton Theorem, eigenvalues of transpose, inverse, Hermitian, quasidiagonal and similar matrices, similarity transformation, diagonalization of a matrix, power method for least eigenvalue, eigenvectors as solutions of homogenous equations.

PART – B

Linear Programming
General formulation of LP problem, simplex method.

Numerical Differentiation and Integration
Numerical differentiation using finite differences, numerical integration, Newton-cotes formulae-Trapezoidal rule for integration, Simpson’s 1/3 rule, Simpson’s 3/8 rule.

Numerical Solutions of Differential Equations
Numerical solutions of first order ordinary differentials equations using Taylor’s series, Picard’s, Euler’s, Modified Euler’s method, Runge-Kutta method of fourth order, Predictor-corrector method (Milne’s method and Adam’s method), choice of method, stability of numerical integration procedure.

BOOKS RECOMMENDED:

SYLLABUS FOR
BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)
SIXTH SEMESTER

Paper Title: - ELECTRONICS SYSTEM DESIGN

Paper Code: EECE 601 Max. Marks: 100 Time: 3 hours

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART-A

1. Review of Digital electronics concept [02]

2. MSI and LSI Circuits and Their Applications [05]

3. Sequential Machines [08]

PART-B


5. Asynchronous Finite State Machines [15]
   Scope, Asynchronous Analysis, Design Of Asynchronous Machines, Cycle And Races, Plotting And Reading The Excitation Map, Hazards, Essential Hazards Map Entered Variable, MEV Approaches To Asynchronous Design, Hazards In Circuit Developed By MEV Method

BOOKS RECOMMENDED:

1. An Engineering Approach to Digital Design - by Fletcher PHI 1990
2. Designing with TTL Circuits - by Texas Instruments.
3. Related IEEE/IEE publications
Paper Title: - MICROWAVES ENGINEERING

Paper Code: EECE -602
Max. Marks: 100
Time: 3 hours

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART - A

Microwave Tubes:
Limitations of conventional tubes, construction, operation and properties of Klystron Amplifier, reflex Klystron, Magnetron, TWT, BWO, Crossed field amplifiers.

Microwave Solid State Devices:
Limitation of conventional solid state devices at MW, Transistors (Bipolar, FET), Diodes(Tunnel, Varactor, PIN), Transferred Electron Devices (Gunn diode), Avalanche transit time effect (IMPATT, TRAPATT, SBD)

PART- B

Microwave Components:
Analysis of MW components using s-parameters, Junctions (E plane, H plane, Hybrid), Directional coupler, Bends and Corners, MW posts, S.S. tuners, Attenuators, Phase shifter, Ferrite devices (Isolator, Circulator, Gyrorator), Cavity resonator, Matched Termination.

Microwave Measurements:
Power measurements using calorimeters and bolometers, Measurement of SWR, Frequency and wavelength Microwave bridges.

BOOKS RECOMMENDED:

1) Microwave devices and circuits: Samuel Liao; PHI
2) Microwave devices and radar engg: M.Kulkarni; Umesh Publications
3) Foundation of Microwave Engg : R.E.Collin; McGraw Hill
4) Microwave Engg: K.C Gupta , PEARSONS EDU
5) Microwave Engg. Passive circuits: Peter A. Rizzi
Paper Title: - : MICROWAVE ENGINEERING LAB

Paper Code: EECE -652  Max. Marks: 40

Note: At least eight experiments are to be done.

List of Experiments:

1. Study of microwave components and instruments.
2. Measurement of crystal characteristics and proof of the square law characteristics of the diode.
8. Calibration of the attenuation constant of an attenuator.
9. Determination of the radiation characteristics and gain of an antenna.
11. Determination of the standing wave pattern on a transmission line and finding the length and position of the short circuited stub.

Paper Title: MICRO CONTROLLER & EMBEDDED SYSTEMS

Paper Code: EECE 603  Max. Marks: 100  Time: 3 hours

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART- A

Introduction:  [03]
8051 Micro controller: Comparison of Microprocessor and Micro-controller, Micro-controller and embedded processors, overview of 8085 families.

8051 Assembly Language Programming:  [07]
Introduction to 8051 Assembly programming, Assembling and running an 8051 program. Data Types and directives. 8051 flag bits and PSW register. Register banks and stack.
Jump loop and call instructions, I/O Port programming: Addressing modes and Accessing memory using various addressing modes. Arithmetic instructions and programs, Logic instructions and programs, Single bit instructions and programming, Timer/counter programming in the 8051

PART - B

Serial Communication: 8051 connection to RS 232, 8051 serial communication programming.

Real World Interfacing: LCD, ADC and sensors, Stepper motor, keyboard, DAC and external memory

Introduction to an embedded system and its design: Introduction to ES & its applications, design parameters of an ES and its significance (With respect to all parameter), present trends in ES, Embedded System design life cycle, product specifications and hardware, software partitioning, Code sign.

Introduction to latest micro controllers such as ARM processors and its applications.

BOOKS RECOMMENDED:


b. David e Simon, “Am embedded software primer”, Pearson Education

c. Frank vahid and Tony Givargus, “Embedded system design, Pearson Education”


Paper Title: - MICRO CONTROLLER & EMBEDDED SYSTEMS

Paper Code: EECE-653  Max. Marks: 40

Note: At least eight experiments are to be done.

List of Experiment

1. Study of 8051/8031 Micro controller kits.
2. Write a program to add two numbers lying at two memory locations and display the result.
3. Write a program for multiplication of two numbers lying at memory location and display the result.
4. Write a program to check a number for being ODD or EVEN and show the result on display.
5. Write a program to split a byte in two nibbles and show the two nibbles on display.
6. Write a program to arrange 10 numbers stored in memory location in Ascending and Descending order.
7. Write a program to find a factorial of a given number.
8. Study of Interrupt structure of 8051/8031 micro controllers.
9. Write a program to show the use of INT0 and INT1.
10. Write a program of Flashing LED connected to port 1 of the Micro Controller
11. Write a program to generate a Ramp waveform using DAC with micro controller.
12. Write a program to interface the ADC.
13. Write a program to control a stepper motor in direction, speed and number of steps.
14. Write a program to control the speed of DC motor.
15. Interfacing of high power devices to Micro-controller port-lines, LED, relays and LCD display.

Paper Title: - VHDL PROGRAMING & TECHNOLOGY
Paper Code: EECE 604

Max. Marks: 100 Time: 3 hours

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART - A
Introduction: [10]
Introduction to Computer-aided design tools for digital systems. Hardware description languages, Introduction to VHDL, Data objects, Classes and data types Operators, Overloading, Logical operators. Types of delays, Entity and Architecture declaration. Introduction to behavioral, dataflow and structural models.

VHDL Statements: [10]
Assignmen statements, sequential Statements and process, Conditional statements, Case statements, Array and loops, Resolution functions, Packages & Libraries, Concurrent statements.

Combinational Circuit Design: [08]
VHDL models and simulation of combinational circuits such as Multiplexers, Encoders, Decoders, Code converters, Comparators, Implementation of Boolean functions etc.

PART - B
Sequential Circuit Design: [05]
VHDL Models and simulation of sequential circuits, Shift registers, Counters etc.
Design of Microcomputer:
Basic components of a computer, Specifications, Architecture of a simple Microcomputer system, Implementation of a simple microcomputer system using VHDL.

Design with CPLDs and FPGAs:
Programmable logic devices: ROM, PLAs, GAL, PEEL,CPLDs and FPGA. Design and implementation using CPLDs and FPGAs

BOOKS RECOMMENDED:


Paper Title : VHDL PROGRAMMING & TECHNOLOGY

Paper Code: EECE-654 Max. Marks; 40

Note: At least eight experiments are to be done.

Combinational Design Exercises

1. Design of Gates
   a. Design of AND gate
   b. Design of OR gate
   c. Design of XOR gate
2. Design of XOR gate using other basic gates
3. Design of 2:1 Mux using other basic gates
4. Design of 2 to 4 Decoder
5. Design of Half-Adder, Full Adder, Half Subtractor, Full Subtractor
6. Design of 3:8 Decoder
7. Design of 8:3 Priority Encoder
8. Design of 4 Bit Binary to Grey code Converter
9. Design of 4 Bit Binary to BCD Converter using sequential statement
10. Design an 8 Bit parity generator (with for loop and Generic statements)
11. Design of 2,s Complementer for 8-bit Binary number using Generate statements

Paper Title:- POWER ELECTRONICS.

Paper Code: - EECE 605 Maxmarks :- 100 Time :- 3 Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART - A

Characteristics of Selected Devices:

(07)
Fast recovery diodes, Schottky diode, SCR, gate trigger and commutation circuits, heat sinks, protection circuits, series and parallel connection of SCRs, Diac, Triac, UJT, Power MOSFETs.

Controlled Rectifier:

(07)
Half wave and full wave with resistive & R-L-E and resistive-inductive loads. Free-wheeling diode, three phase rectifiers, Bridge rectifiers - half controlled and fully controlled.

Inverter, Chopper And Cyclo-converter :

(09)
single phase and three phase inverters, introduction to series and parallel inverters. Mc-murray bedford inverters, principle of chopper operation, control strategies, types of chopper, Jones And Morgan Chopper, cycloconverter: single phase bridge cycloconverter and its advantages and disadvantages

PART - B

Motor Control:

(09)
D.C. and A.C. motor control, reversible drives, closed loop control, commutatorless d.c. motor control.
A.C. Voltage Controllers:

(10)
Types of AC Voltage Controllers, Integral cycle control, single phase voltage controller, Sequence control of AC voltage (Transformer tap changers)

BOOKS RECOMMENDED:

3. P.S. Bimbra, “Power Electronics”, Khanna publishers
4. MGD Rashid, “Power Electronics Circuits Devices and Applications”, PHI, New Delhi

Paper Title:- POWER ELECTRONICS

Paper Code:- EECE 655 Max Marks: 40

Note: At least eight experiments are to be done.

List of Practical:

1. Measurement of the following basic diode characteristics of SCR :
   (a) Forward blocking current V/S Voltage.
   (b) Reverse blocking current V/S Voltage.
   (c) Reverse gate current V/S Voltage.
2. To determine the following Turn on characteristics of SCR :
   (a) Gate trigger current (Firing current).
   (b) Gate trigger voltage.
   (c) Latching current.
   (d) Holding current.
3. Study of SCR triggering circuits and to check the performance of one type of triggering circuits.
4. Study of SCR commutation circuits and to check the performance of one type of commutation circuits.
5. Harmonic analysis of a complex voltage waveform by harmonic analysis.
6. Study of chopper circuits to check performance of one type of chopper circuits.
7. Study of inverter circuits and to check the performance of one type of inverter circuits.
8. Speed control of DC motor by solid state devices.
9. Speed control of induction motor using thyristors.
10. Basic triac characteristics.
11. Study of excitation system of a synchronous generator using thyristors and to find excitation response.

Paper Title: - HUMAN RESOURCES MANAGEMENT.

Paper code:- AS - 606 Max Marks :- 50

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART – A


Job analysis & Design: Job Analysis: Job Description & Job Specification.

Job Satisfaction: Job satisfaction and its importance; Motivation, Factors affecting motivation, introduction to Motivation Theory; Workers’ Participation, Quality of work life.

PART-B

The Compensation Function:
Basic concepts in wage administration, company’s wage policy, Job Evaluation, Issues in wage administration, Bonus & Incentives, Payment of Wages Act-1936, Minimum Wages Act-1961

**Integration:**

Human Relations and Industrial Relations; Difference between Human Relations and Industrial Relations, Factors required for good Human Relation Policy in Industry; Employee Employer relationship; Causes and Effects of Industrial disputes; Employees Grievances & their Redressal, Administration of Discipline, Communication in organization, Absenteeism, Labour Turnover, Changing face of the Indian workforce and their environment, Importance of collective Bargaining; Role of trade unions in maintaining cordial Industrial Relations.


**BOOKS RECOMMENDED:**


6. T.N. Bhagotiwal, “Economics of Labour and Industrial Relations”, Sahitya Bhawan Agra
SYLLABUS FOR
BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)

SEVENTH SEMESTER

Paper Title: DIGITAL COMMUNICATION

Paper Code: EECE-701

Max Marks: 100
Time: 3 Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART-A

Digital Transmission:

(15)

Digital Carrier Line Encoding & Multiplexing Techniques:

(10)
Line Coding & its properties. NRZ & RZ types, (No derivation), HDB and B8ZS signaling, Fundamentals of time division multiplexing, T1 Digital Carrier system, Synchronization and Signaling of T1, TDM, PCM hierarchy, North-American Digital Hierarchy; T1 to T4 PCM TDM system (DS1 to DS4 signals), Bit versus word interleaving, Statistical TDM.

PART-B

Digital Carrier Modulation & Demodulation Techniques:

(20)
Introduction, Information capacity, Shannon Limit for Information capacity, Bit Rate, Baud & M-Ary Encoding, Amplitude Shift Keying (ASK), ASK Spectrum, ASK Modulator, Coherent ASK Detector, Noncoherent ASK Detector, Frequency Shift Keying (FSK), FSK Bit Rate and Baud, Bandwidth and Frequency Spectrum of FSK, FSK Transmitter, Non-coherent FSK Detector, Coherent FSK Detector, FSK Detection using PLL, Binary Phase Shift Keying, Binary PSK Spectrum, BPSK Transmitter, Coherent PSK Detection, Quadrature Phase Shift Keying (QPSK), QPSK Demodulator, Offset QPSK, π/4 QPSK, Comparison of conventional QPSK, Offset QPSK and π/4 QPSK, Quadrature Amplitude Modulation (QAM); 8 QAM & 16 QAM transmitters and receivers, Band Width efficiency, Differential PSK, Constant Envelope Modulation; Minimum Shift Keying (MSK) & Gaussian Minimum Shift Keying (GMSK)

RECOMMENDED BOOKS:


**Paper Title:- DIGITAL COMMUNICATION LAB**

**Paper Code:- EECE-751**  Max. Marks :- 75

Note: At least eight experiments are to be done

**LIST OF EXPERIMENTS**

1. Study of Time Division Multiplexing system.
2. Study of pulse code modulation and demodulation.
3. Study of delta modulation and demodulation and observe effect of slope overload.
4. Study pulse data coding techniques for various formats.
5. Data decoding techniques for various formats.
7. Study of frequency shift keying modulator and demodulator.
8. Study of phase shift keying modulator and demodulator.

Experiments can be performed also on Commsim or MATLAB.

**Paper Title:- DIGITAL SIGNAL PROCESSING**

**Paper code:- EECE-702**  Max. Marks:- 100  Time :- 3 Hrs

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART-A**
Continuous Time Signals:-
Review of Fourier series & Fourier transform, sampling of continuous time signals. (3)

Discrete Time Signals:-
Linear time invariant systems, stability & causality, linear constant coefficient difference equation, convolution, Z-Transform & its properties, inverse z transform, Discrete Fourier transform and its properties, fast Fourier transform, decimation in time and decimation in frequency algorithms. (15)

Digital Filters:-
Frequency domain representation of discrete time systems, systems function, Ideal low pass filter. (03)

PART-B

Design of IIR filters:-
Impulse invariance technique, Bilinear transformation. Design of IIR filters using butter worth, chebyshev and elliptic filter digital frequency transformation. (07)

Design of FIR filters-
Window technique, frequency sampling technique, equiripple, approximate technique, comparison of FIR and IIR filters. (08)

Realization of Digital systems:-
Block diagrams and signal flow graphs for FIR and IIR systems. Direct form, cascade and parallel form for IIR. (09)

BOOKS RECOMMENDED:


Paper Title:-DIGITAL SIGNAL PROCESSING

Paper Code:- EECE- 752 Max Marks:- 75

Note: At least eight experiments are to be done

LIST OF EXPERIMENTS

1. Hands on experience on MATLAB
2. Hands on experience on DSP training kits.
3. Obtain Fourier transform of an analog signal.
4. Obtain discrete Fourier transform of a finite duration signal.
5. Design on IIR low pass filter using butter worth technique.
6. Design FIR low pass filter.
7. Display filtered signals in time domain.
8. Determine the spectral characteristics of speech.

Paper Title: WIRELESS AND MOBILE COMMUNICATION

Paper Code: EECE-703 Max. Marks: 100 Time: 3 Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART-A

1. Introduction:-(10)

2. Modulation Techniques:- (11)
Digital Modulation for Mobile radio, Analysis under fading channel, diversity techniques and Rake demodulator. Introduction to Spread Spectrum Communication Multiple Access Techniques used in Mobile Wireless Communications: FDMA/TDMA/CDMA.

PART-B

3. Wireless Networking:- (12)

4. Wireless Standards:- (12)
Wireless standards-GSM, IS-95, UMTS-IMT-2000, Signaling, Call Control, Mobility Management and location Tracing

BOOKS RECOMMENDED:


5. Stallings, Wireless Communication and Networks


8. Related IEEE/IEE publications

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**Paper Title:- NEURAL NETWORKS AND FUZZY LOGIC(ELECTIVE)**

**Paper Code: - EECE 704**

Max. Marks:- 100   Time:- 3Hrs

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

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**PART-A**

**Neural Networks Characteristics:**

(08)


**Basic learning laws:**

(05)

Hebb’s rule, Delta rule, Widrow and Hoff LMS learning rule, correlation learning rule, instar and outstar learning rules.

**Unsupervised Learning:**

(05)

Competitive learning, K-means clustering algorithm, kohonen’s feature maps.

**Radial Basis Function Neural Networks:**

(05)

Recurrent networks, Real Time Recurrent, and learning algorithm.

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**PART-B**

**Introduction to Counter Propagation Networks:**

(06)

CMAC network, ART networks.
Applications of neural nets such as pattern recognition:

(06)
Optimization, control, speech and decision-making.

Fuzzy Logic:

(10)
Basic concepts of Fuzzy Logic, Fuzzy VS Crisp Set, Linguistic variables, membership functions, operations of fuzzy sets, Fuzzy IF-THEN rules, variable inference techniques, defuzzification techniques, basic fuzzy inference algorithm, applications of fuzzy logic, fuzzy system design, implementation of fuzzy system, useful tools supporting design.

BOOKS RECOMMENDED:

2. Yegna Narayanan, "Artificial Neural Networks".
3. Bart Kosko, "Neural Networks and Fuzzy Logic".
4. Simon Haykin, "Neutral Networks".
5. Yen and Langari, “Fuzzy Logic: Intelligence, Control and Information”, Pearson Education India.

Paper Title: ARTIFICIAL INTELLIGENCE

Paper Code:EECE 704 Max. Marks:- 100 Time :- 3Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART-A

Introduction:

(03)
The importance of AI, Early work in AI, AI and related fields, introducing intelligence in the methods of attack, criteria for success.

Problem Solving:

(08)

Knowledge Representation:

(08)
Definition and importance of knowledge, representing single facts in logic, resolution non-monotonic reasoning, Dealing within inconsistencies and uncertainties, Fuzzy logic, Bayesian probabilistic interference, dempster shafer theory, Ad-Hoc methods, Heuristic reasoning methods, structural representation of knowledge graphs, frames and related structures.

PART-B

Natural Language Processing:-

Overview of Linguistics, Grammars and Languages, Basic Paying Techniques, Semantic Analysis and Representation Structures, Natural language generation, natural system.

(10)

Pattern Recognition:-
Recognition and classification process, learning classification patterns, recognizing and understanding speech.

(10)

Expert System:-

Rule based system architectures, model based system, constraint satisfaction dealing with uncertainties, knowledge acquisition and validation expert system building tools. Introduction to neural networks, learning algorithms and models.

(06)

BOOKS RECOMMENDED:

1. Dan W. Patterson, Introduction To Artificial Intelligence and Expert System, PHI.


Paper Title:- WEB TECHNOLOGIES

Paper Code:- EECE 704 Max. Marks:- 100 Time :- 3Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART- A

Internet And World Wide Web: -

Introduction, Internet Addressing, ISP, types of Internet Connections, Introduction to WWW, WEB Browsers, WEB Servers, URLs, http, WEB applications, Tools for WEB site creation.

HTML:-

Introduction to HTML, Lists, adding graphics to HTML page, creating tables, linking documents, frames, DHTML and Style sheets

(06)

(06)
**Java Script:**
Introduction, programming constructs: variables, operators and expressions, conditional checking, functions and dialog boxes, JavaScript DOM, creating forms, introduction to Cookies.

**PART B**

**Java:**
Introduction to java objects and classes, control statements, arrays, inheritance, polymorphism, Exception handling, Multithreading. Building the Java Applets, Boxes, Radio Button, Managing Multiple controls, Scrollbars, Choice controls, Scrolling lists, Windows, Menu and Dialog Boxes, Pop up Windows, Graphics in Java, Mouse events, Drawing Objects, Fonts, Canvases, Images, Image maps, Graphics, Animation.

**XML:**
Why XML, XML syntax rules, XML elements, XML attributes, XML DTD displaying XML with CSS.

**BOOKS RECOMMENDED**

3. Web Enabled Commercial Application Development, by Ivan Bayross, BPB.

**Paper Title:** RADAR ENGINEERING

**Paper code:** EECE 704
Max. marks: 100
Time: 3 Hrs

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART-A**

**Introduction to Radar Systems**
Radar equation, FM-CW radar, altimeter, MTI, pulse Doppler radar. Tracking radar-lobe switching, conical scan, mono-pulse, FM pulse compression radar. SAR, ECCM.

**PART-B**

**Radar Antennas**

Paraboloid, lenses, cosecant squared antenna.

**Navigation:**

(18)
Loop antenna, automatic direction finder, radio range, TACAN, ILS, GCA, Microwave landing System, LORAN & DECCA, Missile guidance and seeker systems.

**BOOKS RECOMMENDED:**


**Paper Title:- SEMINAR 1**

**Paper Code:- EECE-753**

Seminar topics to be allotted by teacher concerned based on the latest topic in the subject concerned.

**Paper Title:- MINOR PROJECT**

**Paper Code:- EECE -754**

Max Marks:- 100
SYLLABUS FOR
BACHELOR OF ENGINEERING (ELECTRONICS AND ELECTRICAL COMMUNICATION)
EIGHTH SEMESTER

Paper Title: - OPTICAL FIBER COMMUNICATIONS

Paper code: EECE 801 Max. Marks :- 100 Time:- 3Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART-A

Introduction:

Optical Fibers:

PART-B

Optical Transmitters:

Optical Receivers:

Multi channel Systems:
WDM Light wave systems, Optical TDM Systems, Subscriber Multiplexing, Code Division Multiplexing.

BOOKS RECOMMENDED:

2. Senior J. Optical Fiber Communications, Principles & Practice, PHI.
Paper Title:- OPTICAL FIBER COMMUNICATIONS

Paper Code: EECE 851  
Max. Marks :- 25

Note: At least eight experiments are to be done

1. To determine the Numerical aperture of a given fiber and losses in optical fiber.
2. To determine the V. Parameter the core radius and core cladding dielectric constant difference of a Step Index Single Mode fiber.
3. To measure the cut off wave length of a single mode fiber.
4. To study fiber optical analog link.
5. To study fiber optical digital link.
6. To study the effect of EMI/RFI on an optical fiber medium.
7. To study the effect of pulse broadening on the bandwidth of a fiber optical link.
8. To set up the multiplexer and observe the simultaneous transmission of several channels on fiber optical link.
9. To study Manchester coding/decoding of fiber optical link.
10. To study the linearized A-Law PCM coding on fiber optical link.
11. To study laser communication system.
12. To set up digital optical link using PC.
13. To study various characteristics of fiber using PC.
14. Use of connectorisation kit.
15. To study the following instruments:
   (a) Fiber optical power meter.
   (b) Fiber optical power source.

Paper Title:- COMPUTER NETWORK

Paper Code: - EECE 802  
Max. Marks :- 100  
Time:- 3Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART-A

Brief Introduction:
-232c and RS-449 switching circuits, virtual circuits, Narrow band, ISDN.

Data Link Layer:
Design issues, Elementary data link protocols, sliding window protocols, protocol specifications, Data link layer in the internet and ATM.

Medium Access Sub Layer:
Channel allocation problems, ALOHA, Carrier Sense Multiple Access Protocol, CSMA/CD, CDMA
PART-B

Network Layer:
Design issues, Routing Algorithm, congestion control algorithm Internet working, the network layer in the Internet.

Transport Layer:
Services, protocols, Performance issues.

Application Layer:

BOOKS RECOMMENDED:
Computer Networks by Andrew S. Tanenbaum (3rd Edition), PHI.

Paper Title:- COMPUTER NETWORKING
Paper Code:- EECE 852 Max. Marks :- 25
Note: At least eight experiments are to be done

1. To study different connecting cables and their comparisons.
2. To study sharing and transfer of data in local area network.
3. To study the ping commands and its utilities.
4. To study the remote login in computer system.
5. To configure a single pc as a router.
6. To examine the differences VLAN and LAN.
7. To plan a network in a organization
8. To study IP configuration.
9. To study netstat, all commands.

ELECTIVES

Paper Title:- DIGITAL IMAGE PROCESSING
Paper Code:- EECE 803 Max Marks:- 100 Time:- 3Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART A

Introduction
Fundamental Steps in Image Processing, Elements of Digital Image Processing, Image Acquisition, Storage, Processing, Communication, Display.
**Image Perception**  
Structure of the human eye, light, luminance, brightness, contrast, image model, sampling and quantization-uniform and non uniform, basic relationships between pixels, imaging geometry, camera model, stereo imaging.

**Image Enhancement**  
Spatial domain methods, Frequency domain methods, Enhancement by point processing, histogram processing, image subtraction, image averaging, spatial filtering, smoothing filters, sharpening filters, Enhancement in the frequency domain, Color image processing.

**PART B**

**Image Transforms**  

**Image Compression**  

**BOOKS RECOMMENDED**


**Paper Title: - SATELLITE COMMUNICATION**

**Paper Code: - EECE 803**  
Max. Marks: - 100  
Time: -

3Hrs

**Note for paper setter:** Total of *Eight* questions may be set covering the whole syllabus taking *four* from Part A & *four* from Part B. Candidates will be required to attempt any *five* questions taking at least *two* from each Part.

**PART A**

**Introduction:**  
**Communication Satellite Link Design:**
Introduction, general link design equation, System noise temperature, C/N & G/T ratio, atmospheric & ecorespheric effects on link design, complete link design, interference effects on complete link design earth station Parameters.

**Satellite analog & digital communication:**

**PART-B**

**Multiple Access Techniques:**
TDMA frame structure, burst structure, frame efficiency, Super frame, frame acquisition & synchronization, TDMA vs. FDMA, burst time plan, Beam hopping, satellite switched, Erlang call congestion formula, demand assignment Ctrl, DA - FDMA system, DA - TDMA.

**Satellite Applications:**
Satellite TV, telephone services via satellite, Data Communication services and satellites for earth observation, weather forecast, military appliances, scientific studies.

**BOOKS RECOMMENDED:**


**Paper Title:- NANO TECHNOLOGY**

**Paper Code: EECE 803**

Max. Marks:- 100  Time:- 3Hrs

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

**PART A**
**Introduction to Physics of the Solid State:**

**Properties of Individual Nanoparticles:**
Introduction to Semiconducting Nanoparticles, Introduction to Quantum Dots, wells, wires, Preparation of Quantum Nanostructures, Introduction to Carbon Nanotubes, Fabrication, Structure, Electrical properties, Vibrational properties, Mechanical properties.

**Biological Materials:**

Biological Building Blocks, Nucleic Acids, Biological Nanostructures.

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**PART B**

**Tools:**
TEM, Infrared and Raman Spectroscopy, Photoemission and X-RAY spectroscopy, Electron microscopy, SPMs, AFMs, Electrostatic force Microscope, Magnetic force microscope

**Nanoscale Devices:**
Introduction, Nanoscale MOSFET-planer and non planer, Resonant-tunneling diodes, Single electron transistor, Quantum-Dot, Nano-electrochemical systems, Molecular/Bimolecular electron devices,

**Reference Books:**
1. Nanotechnology: G.Timp, Bell Labs, Murray Hill, NJ(Ed.)
2. Introduction to Nanotechnology-Charless P. Poole, Wiley International

**Paper Title: - COMPUTER ARCHITECTURE**

**Paper Code: EECE 804**

**Max. Marks:- 100**

**Time:-**

3 Hrs

**Note for paper setter:** Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

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**PART-A**
Basic Computer Organization and Design:
Set of Computer Instructions, Registers, timing and Control Signals, flow charts for instruction cycle, flow charts for interrupt cycle, Design of hard wired control unit, control unit, control memory, Design of micro-programmes control unit.

Central Processing Organization:
Processor bus organization Arithmetic Logic Unit (ALU)

Arithmetic Processor Design:
Addition and subtraction of unsigned binary numbers, Addition and subtraction Algorithm for signed binary numbers, Multiplication Algorithm, Division algorithm for signal and unsigned binary numbers, Floating Point Arithmetic Operations.

PART-B

Memory Organization:
Memory technology, address mapping in RAM & ROM, memory Hierarchies, virtual memory, cache memory, Interleaved and Associative memories, memory management unit, hard disk drive, floppy disk drive and CD-ROM.

Parallel Processing
Types of parallel processors, performance considerations, pipeline processors, multiprocessors, Array processors.

BOOKS RECOMMENDED:


Paper Title:- VLSI DESIGN

Paper Code:- EECE 805
Max Marks:- 100
Time: 3 Hrs

Note for paper setter: Total of Eight questions may be set covering the whole syllabus taking four from Part A & four from Part B. Candidates will be required to attempt any five questions taking at least two from each Part.

PART - A

1. Introduction to MOS Technology:
   Enhancement & depletion mode transistors.

2. MOS Transistors:
   Parameters pass transistor, NMOS inverters, CMOS Inverters, MOS Transistor circuit model,
   Latch up in CMOS circuits, Basic gates, Depletion & enhance mode pull ups.
3. **MOS Circuit Design Processes:**
MOS layers stick diagrams, design rules and layout.

4. **Basic circuit concepts:**
Sheet resistance concept applied to MOS transistors and Inverters Area Capacitance of layers,
Inverter delays, Super buffers, propagation delays.

**PART-B**

5. **Subsystem Design and Layout:**
Switch logic, gate logic, inverter, two input NMOS, CMOS and BICMOS NAND and NOR gates,
Design of Combinational Circuits, PLA Design of Sequential Circuits—two phase clock dynamic
shift registers, register to register transfer, Finite State Machines.

6. **Implementing Integrated System Design:**
Patterning and fabrication, hand layout and digitization using a symbolic layout language, the
Caltech immediate form for LSI layout description, the multi-project chip.

7. **Overview of an LSI Computer System and Design of OM2 Data Path Chip:**
System overview, overall structure of data path, ALU, ALU register, Buses, Shifter, Array etc.

**BOOKS RECOMMENDED:**

3. VLSI Design by Pucknell

**Paper Title:- SEMINAR-2**

**Paper Code:- EECE 855**

Seminar topics to be allotted by teacher concerned based on the latest topic in the subject concerned.

**Paper Title:-MAJOR PROJECT**

**Paper code:- EECE 854**

Max. Marks:- 100

Project topics to be allotted by guide concerned.